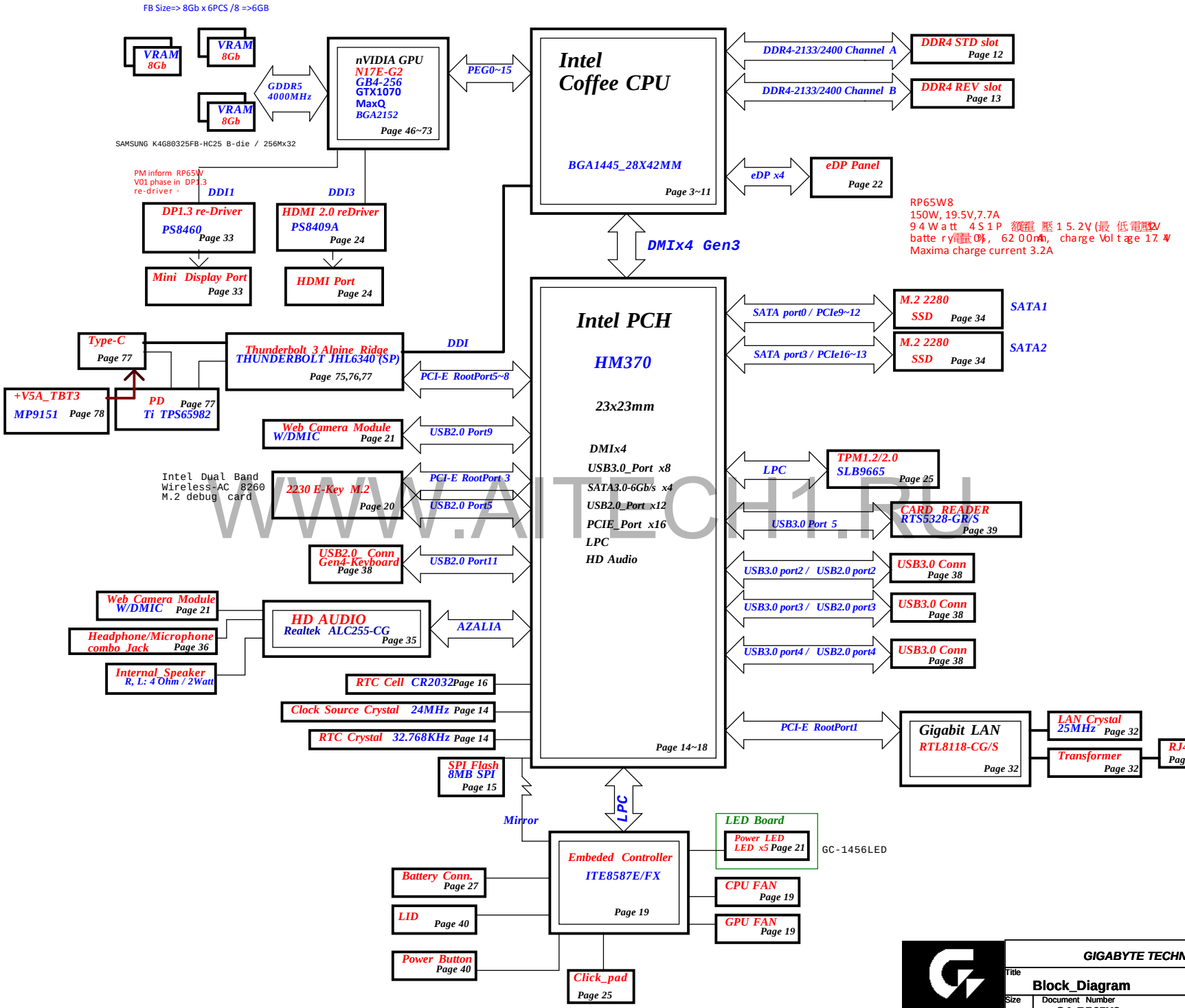

Note:

ALC255 copy from RP64

GIGABYTE TECHNOLOGY COPORATION

Title: Block_Diagram

Size | Document Number: GA-RP65X8 | Rev: 1.0

Date: Thursday, February 01, 2018 | Sheet 1 of 78

Circuit, PCB, Layout ..etc Change Note

Rev.	Page	Change Item	Reason	Layout
0.1	32	RTL8118AS-CG change to RTL8118-CG del L1012,C1249 and C1243 add R711296 and C8007		L
	15	PCIE 20 and 19 port P & N change		L
	6	del CR66,CR27 ADD CR67,CR39,CR16 CR 23 change to 20 ohm		
	14	PR1475 pull high +V3.3A_DSW		L
	6	del CR68,CR69		L
	6	Del RT9018A-25PSP ; Add RT8068AZQW		
1.0	15	PR6 , PR7 , PR8 , PR10 , PR11 , PR13 Resistor from 15 ohm change to 0 ohm		
	17	Remove RP161 , RP165 , RP170		
	27	CHR26 Resistor from 232K ohm change to 165K ohm		
	38	R711285 , R711289 , R711293 Resistor from 47K change to 52.3K Remove R71317 , R71319 , R71315 , R71321 , R711364 , R711362 R71313 add resistor 0 ohm		
	28	R71201 mount 100 ohm and Q7120 mount QN7002 MOS.		
	41	IR47 and IR6 resistor from 3.83K change to 7.15K		

Rev.	Page	Change Item	Reason	Layout

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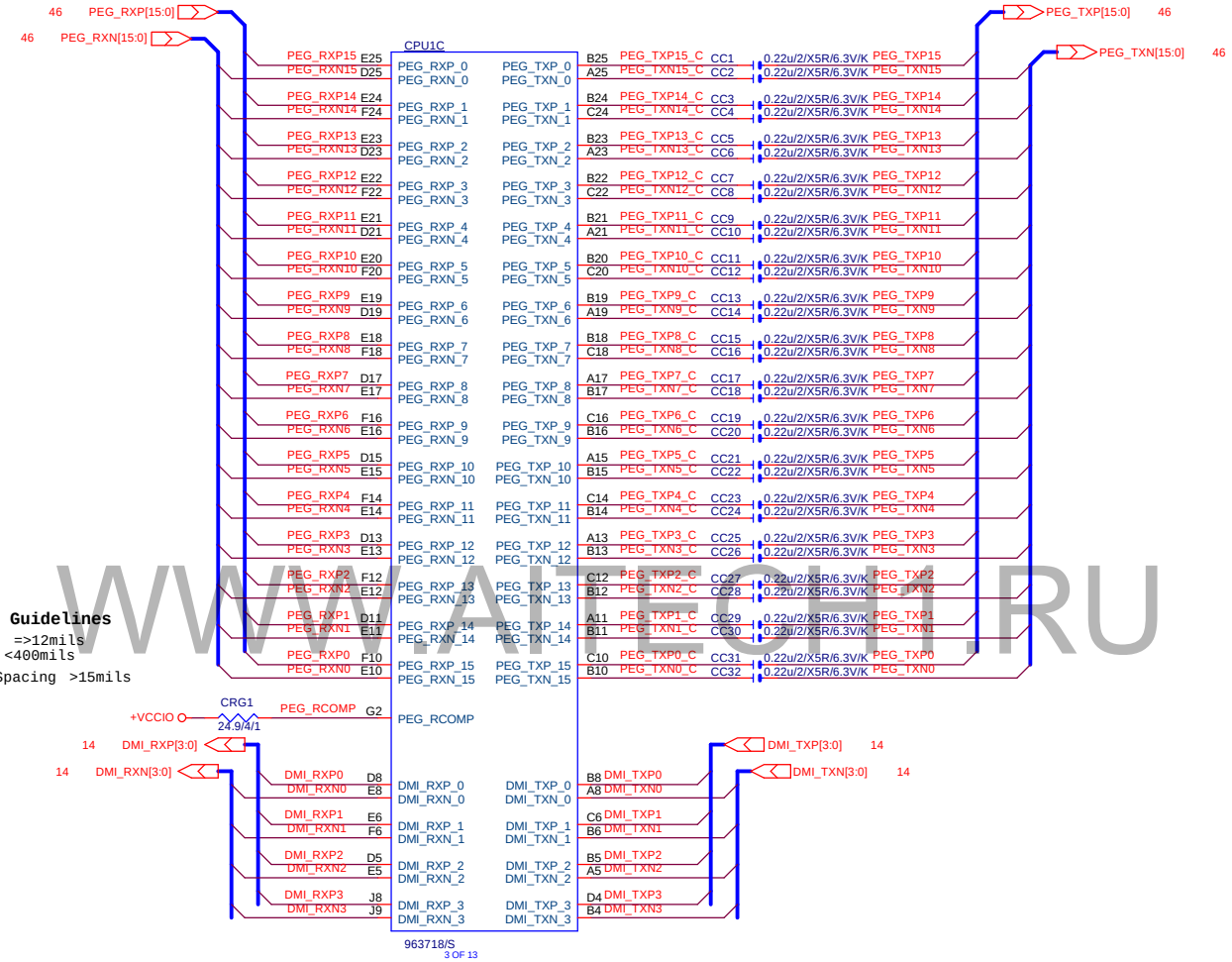
Title: Change_Note

Size | Document Number: GA-RP65X8 | Rev: 1.0

Date: Thursday, February 01, 2018 | Sheet 2 of 78

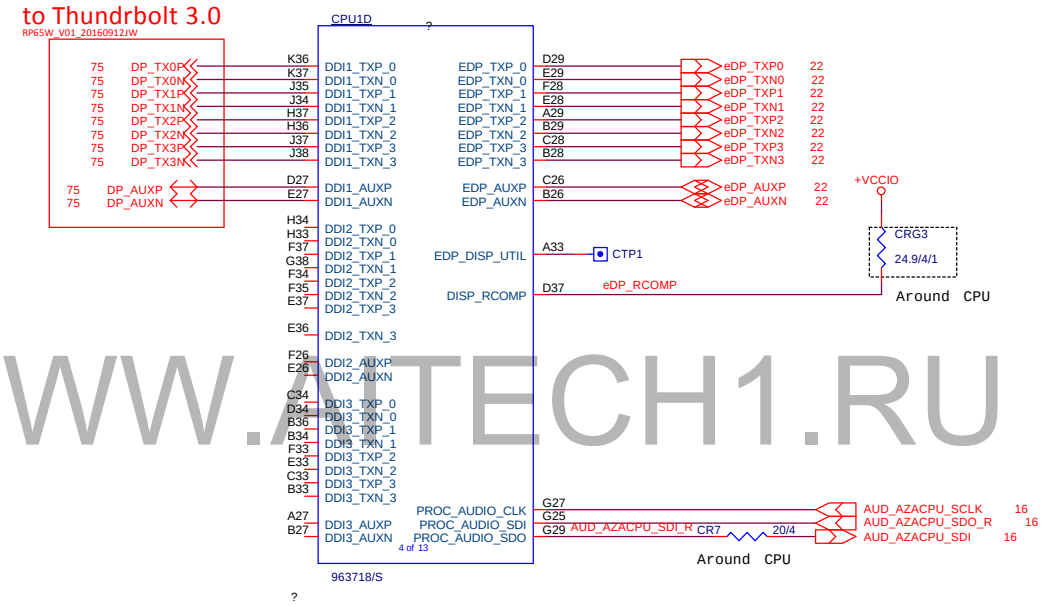


PEG_RCOMP Guidelines

Trace Width =>12mils
Max Length <400mils

Min Trace Spacing >15mils

GIGABYTE	GIGABYTE TECHNOLOGY COPORATION	
	Title: CPU_1-PEG	
	Size	Document Number: GA-RP65X8 — Rev: 1.0
	Date: Thursday, February 01, 2018	Sheet 3 of 78



eDP_RCOMP Guidelines

Trace Width =>12mils
Max Length <100mils
Min Trace Spacing >25mils

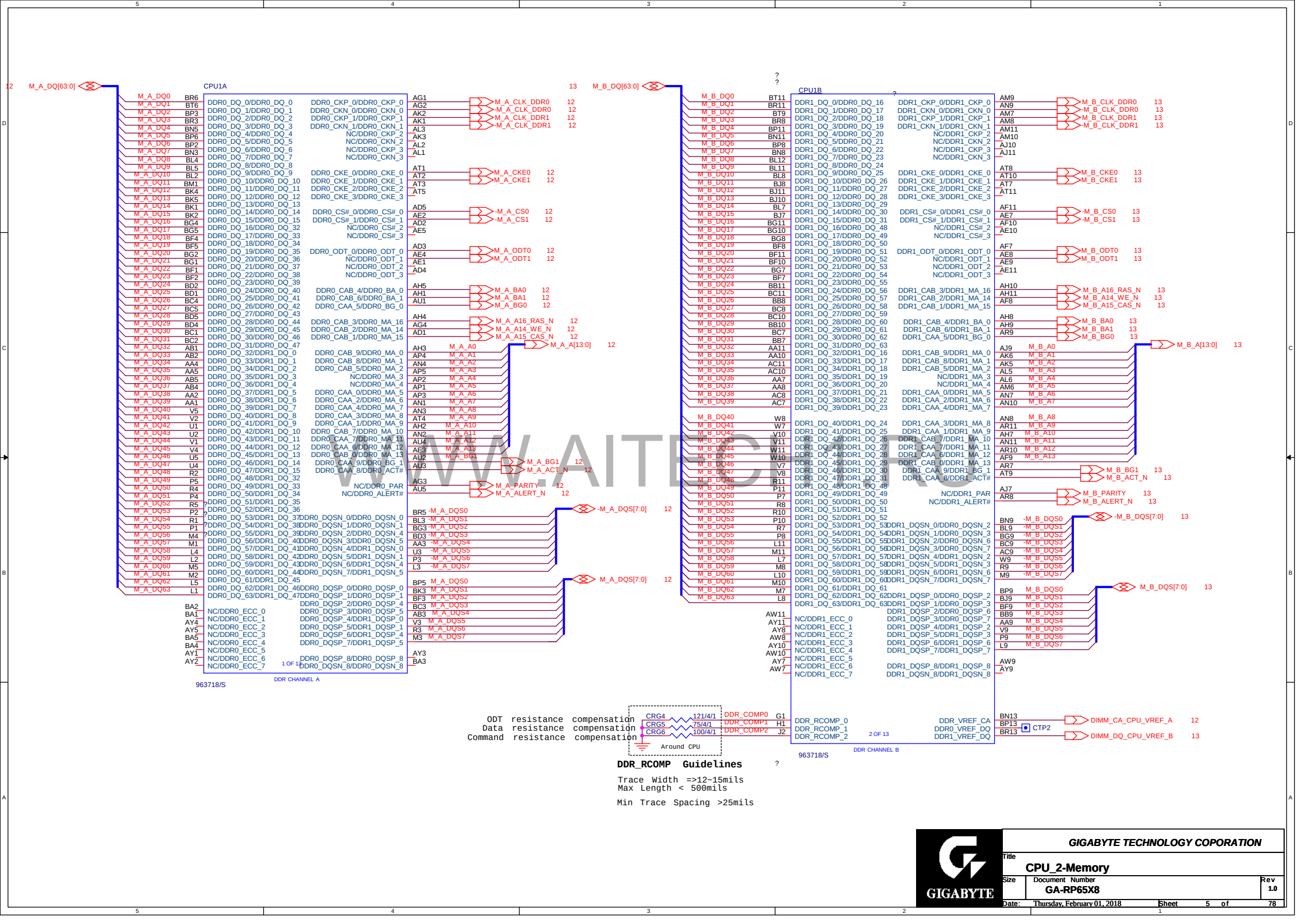
GIGABYTE

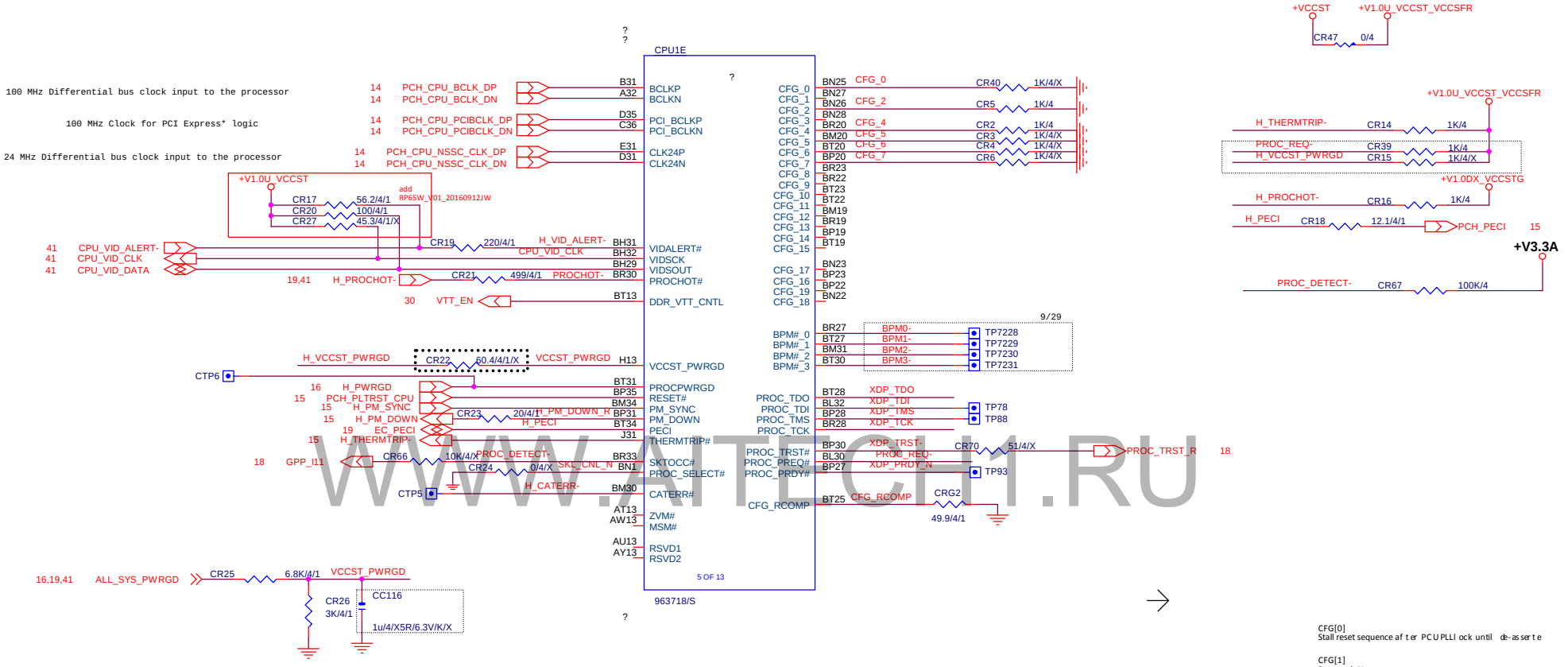
GIGABYTE TECHNOLOGY COPORATION

Title: CPU_3-DDI

Size | Document Number: GA-RP65X8 | Rev: 1.0

Date: Thursday, February 01, 2018 | Sheet 4 of 78


CPU1A
CPU1B
M_A_DQ[63:0]
M_B_DQ[63:0]
DDR CHANNEL A
DDR CHANNEL B
963718/S
1 OF 13
2 OF 13
ODT resistance compensation
Data resistance compensation
Command resistance compensation
Around CPU
DDR_RCOMP Guidelines
Trace Width =>12~15mils
Max Length < 500mils
Min Trace Spacing >25mils
GIGABYTE TECHNOLOGY COPORATION
CPU_2-Memory
GA-RP65X8
Thursday, February 01, 2018
Sheet 5 of 78



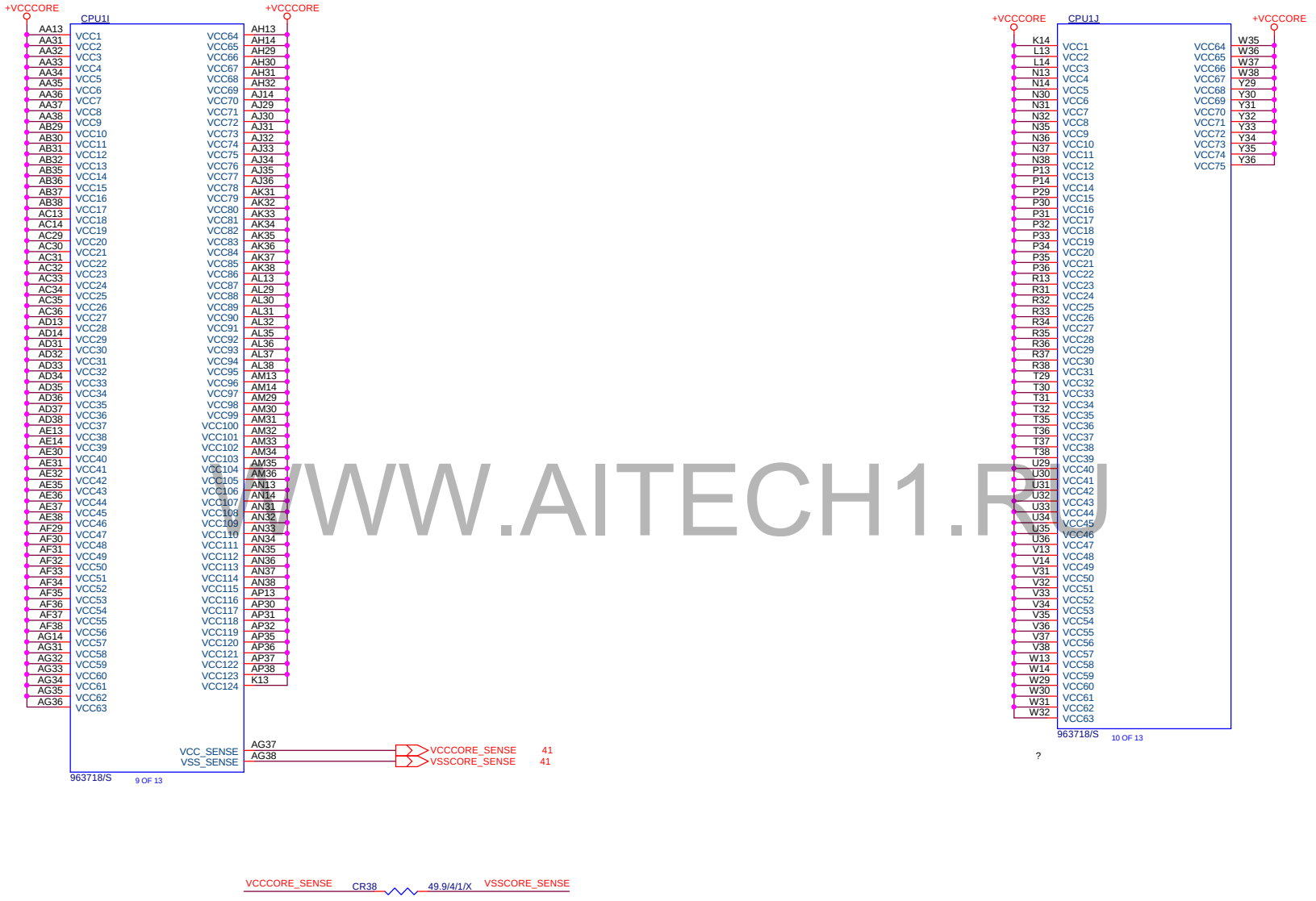
GIGABYTE

GIGABYTE TECHNOLOGY COPORATION

Title: CPU_3-NOA/JTAG/MISC

Size: | Document Number: GA-RP65X8 | Rev: 1.0

Date: Thursday, February 01, 2018 | Sheet 6 of 78



[PAGE_TITLE=CPU SYMBOL - 7 ,10 OF 11 (CPU POWER- 1 OF 3)]

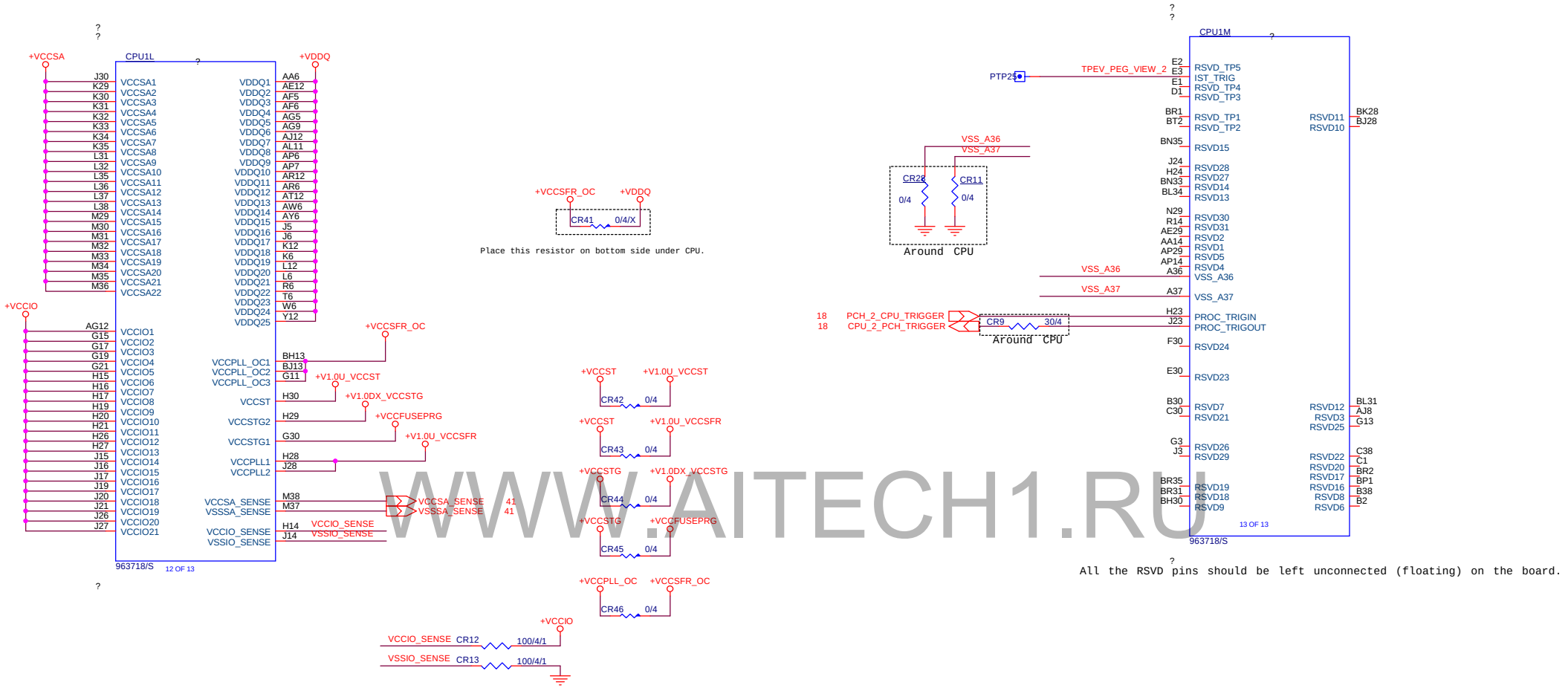
GIGABYTE

GIGABYTE TECHNOLOGY COPORATION

Title: CPU_4-VCC/VDDQ

Size | Document Number: GA-RP65X8 | Rev: 1.0

Date: Thursday, February 01, 2018 | Sheet 7 of 78



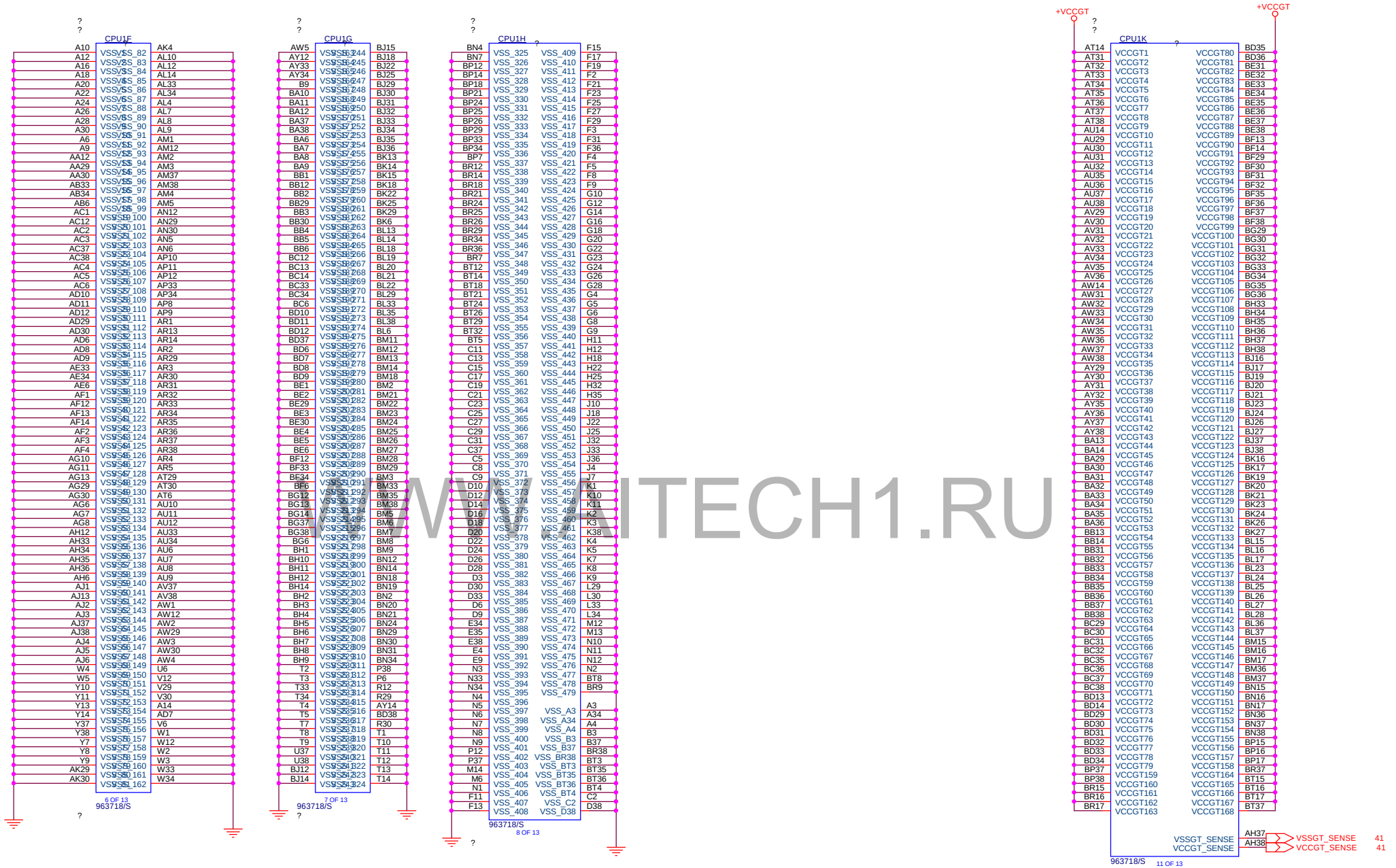
GIGABYTE

GIGABYTE TECHNOLOGY COPORATION

Title: CPU_6-POWER 2 OF 3

Size | Document Number: GA-RP65X8 | Rev: 1.0

Date: Thursday, February 01, 2018 | Sheet 8 of 78

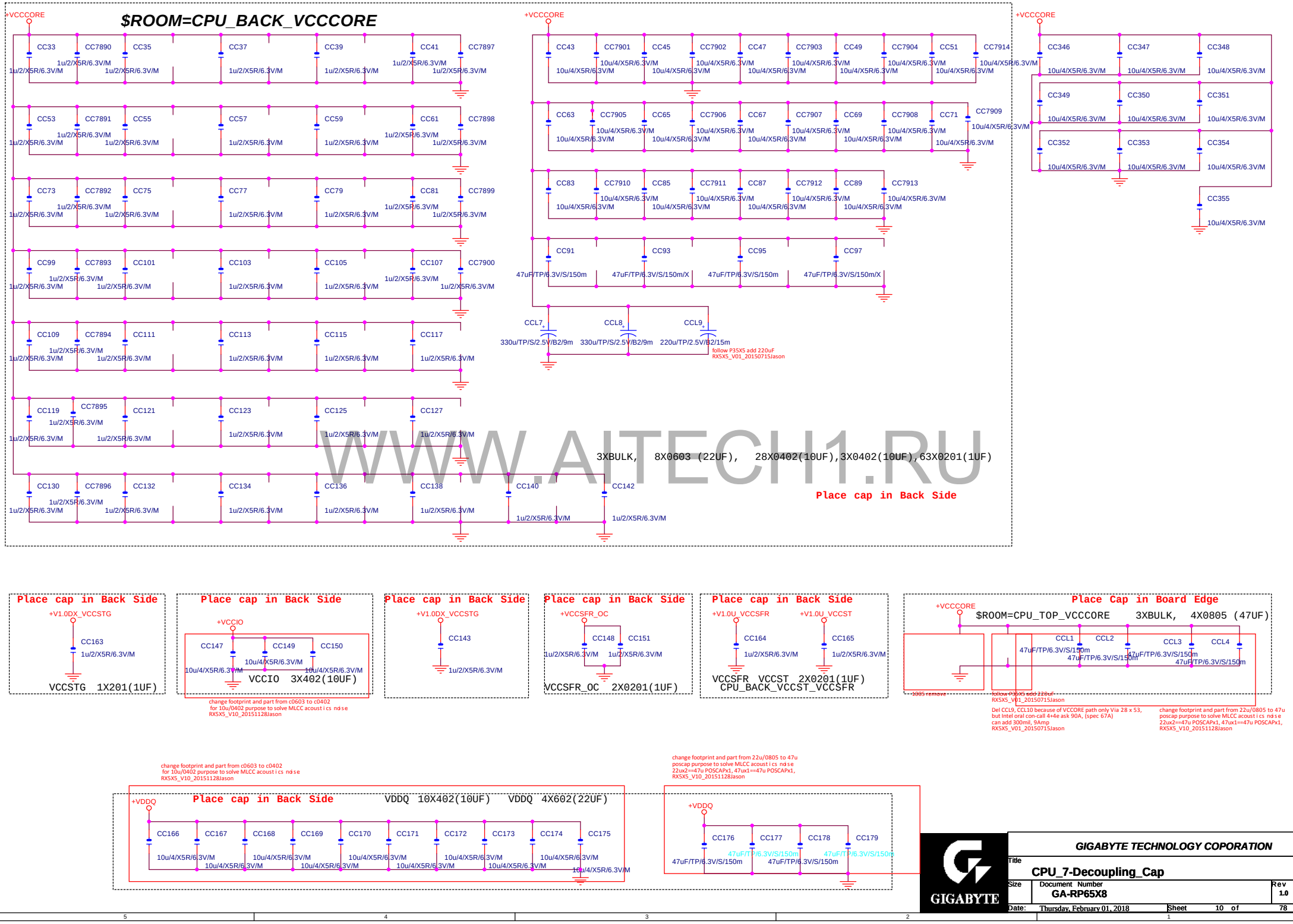


GIGABYTE TECHNOLOGY COPORATION

Title: CPU_7-POWER 3 OF3

Size | Document Number: GA-RP65X8 | Rev: 1.0

Date: Thursday, February 01, 2018 | Sheet 9 of 78



1X0805(47UF), 7X0402(10UF), 3X0201(1UF)

Place cap in Back Side

+VCCSA

CC180 47uF/TP/6.3V/S/150m

CC181 47uF/TP/6.3V/S/150m

CC183 47uF/TP/6.3V/S/150m/X

CC185 10u/4/X5R/6.3V/M

CC187 10u/4/X5R/6.3V/M

CC188 1u/2/X5R/6.3V/M

CC189 1u/2/X5R/6.3V/M

CC190 1u/2/X5R/6.3V/M

20150612 AE informs ISL95855 量產測項(Change the output capvalue is for intel VTT DMM 調整設定的切換頻率較高(700KHZ)，pcap放電太慢要改MLCC)建議修改+VCCGT & +VCCSA電容輔較應速度較快，change ICL19 330uF to 47uF x2, ICL18 330uF to 220uF ICL15 330uF to 220uF CC181 10uF to 22uF, CC183 10uF to 22uF RX5K5_V01_20150617Jason

change footprint and part from 22u/0603 to 47u poscap purpose to solve MLCC acoustics noise 22ux2==47u POSCAPx1 47ux1==47u POSCAPx1 RX5X5_V10_20151128Jason

change footprint and part from c0603 to c0402 for 10u/0402 purpose to solve MLCC acoustics noise RX5X5_V10_20151128Jason

Place Cap in Board Edge

$ROOM=CPU_TOP_VCCSA

CCL14 47uF/TP/6.3V/S/150m

change footprint and part from 22u/0805 to 47u poscap purpose to solve MLCC acoustics noise 22ux2==47u POSCAPx1, 47ux1==47u POSCAPx1, RX5X5_V10_20151128Jason

1005 remove

2XBULK , 1X0805(22UF)

CC356 10u/4/X5R/6.3V/M

CC357 10u/4/X5R/6.3V/M

CC358 10u/4/X5R/6.3V/M

CC359 10u/4/X5R/6.3V/M

add more 4EA for common circuit RX5X6_V02_20160427J

remove 4+4e RX5X5_N17_V01_20160125

change footprint and part from 22u/0805 to 47u poscap purpose to solve MLCC acoustics noise 22ux2==47u POSCAPx1, 47ux1==47u POSCAPx1, RX5X5_V10_20151128Jason

Place Cap in Board Edge

CCL16 330u/TP/S/2.5V/B2/9m

CCL17 330u/TP/S/2.5V/B2/9m

CC215 47uF/TP/6.3V/S/150m

CC216 47uF/TP/6.3V/S/150m

CC217 47uF/TP/6.3V/S/150m

CC218 47uF/TP/6.3V/S/150m

CC219 47uF/TP/6.3V/S/150m

CC220 47uF/TP/6.3V/S/150m

4XBULK, 6X0805(47UF)

change +VCCGT cap NA, discrete no need RX5X6_V10_20160702J

add +VCCGT cap components back RX5X6_V10_BOM10D_20160810J

add +VCCGT cap components back RX5X6_V10_BOM10D_20160810J

change +VCCGT cap NA, discrete no need RX5X6_V10_20160702J

3XBULK (SMC7343D), 8X0603(22UF), 35X0402 (10UF), 68X0201 (1UF)

CC226 1u/4/X5R/6.3V/K

CC228 1u/4/X5R/6.3V/K

CC230 1u/4/X5R/6.3V/K

CC232 1u/4/X5R/6.3V/K

CC234 1u/4/X5R/6.3V/K

CC246 1u/4/X5R/6.3V/K

CC248 1u/4/X5R/6.3V/K

CC250 1u/4/X5R/6.3V/K

CC252 1u/4/X5R/6.3V/K

CC254 1u/4/X5R/6.3V/K

CC266 1u/4/X5R/6.3V/K

CC268 1u/4/X5R/6.3V/K

CC270 1u/4/X5R/6.3V/K

CC272 1u/4/X5R/6.3V/K

CC274 1u/4/X5R/6.3V/K

Place cap in Back Side

CC236 10u/4/X5R/6.3V/M

CC238 10u/4/X5R/6.3V/M

CC240 10u/4/X5R/6.3V/M

CC242 10u/4/X5R/6.3V/M

CC244 10u/4/X5R/6.3V/M

CC256 10u/4/X5R/6.3V/M

CC258 10u/4/X5R/6.3V/M

CC260 10u/4/X5R/6.3V/M

CC262 10u/4/X5R/6.3V/M

CC264 10u/4/X5R/6.3V/M

CC291 47uF/TP/6.3V/S/150m

CC293 47uF/TP/6.3V/S/150m/X

CC295 47uF/TP/6.3V/S/150m

CC297 47uF/TP/6.3V/S/150m/X

change footprint and part from 22u/0805 to 47u poscap purpose to solve MLCC acoustics noise 22ux2==47u POSCAPx1, 47ux1==47u POSCAPx1, RX5X5_V10_20151128Jason

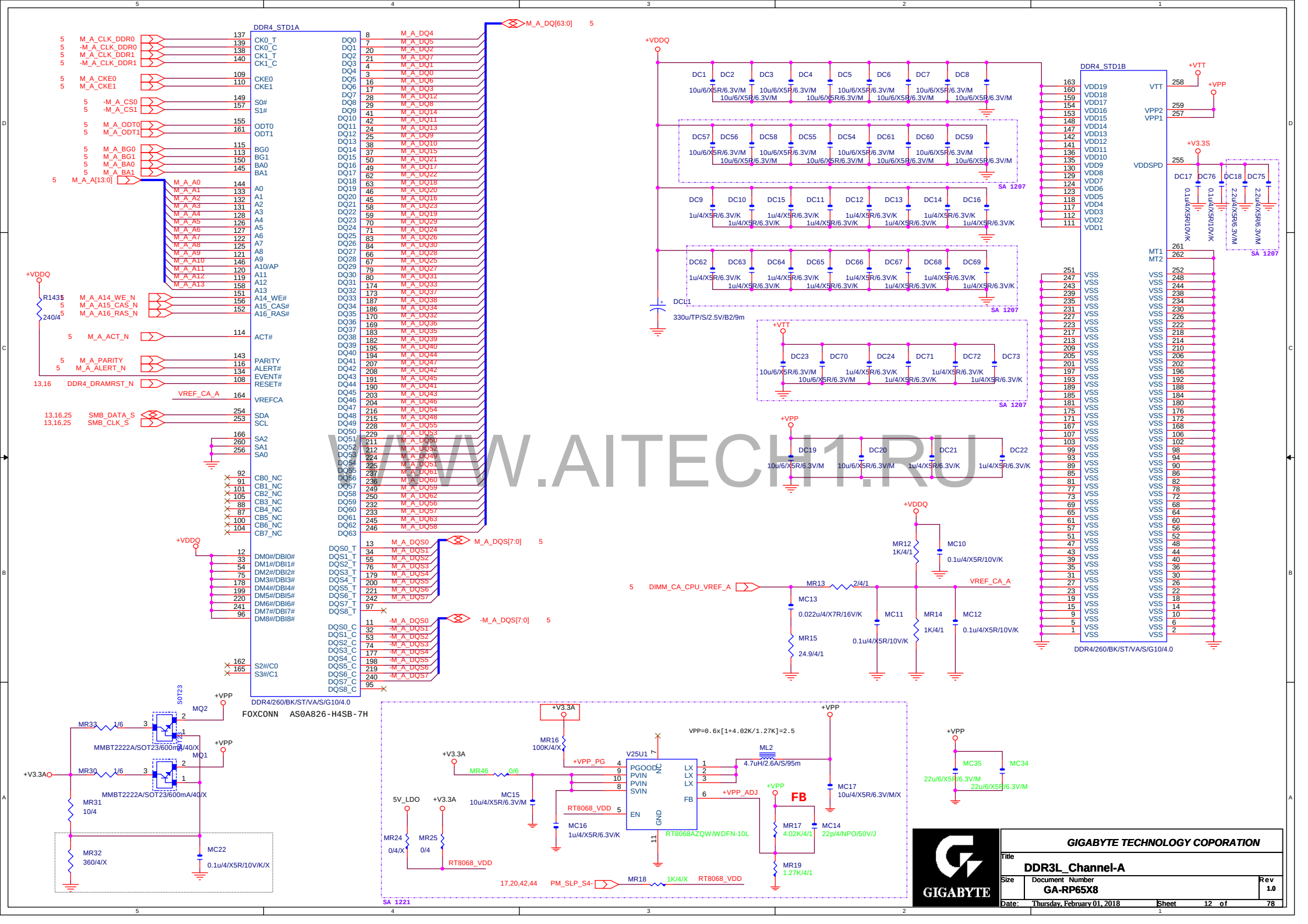
GIGABYTE

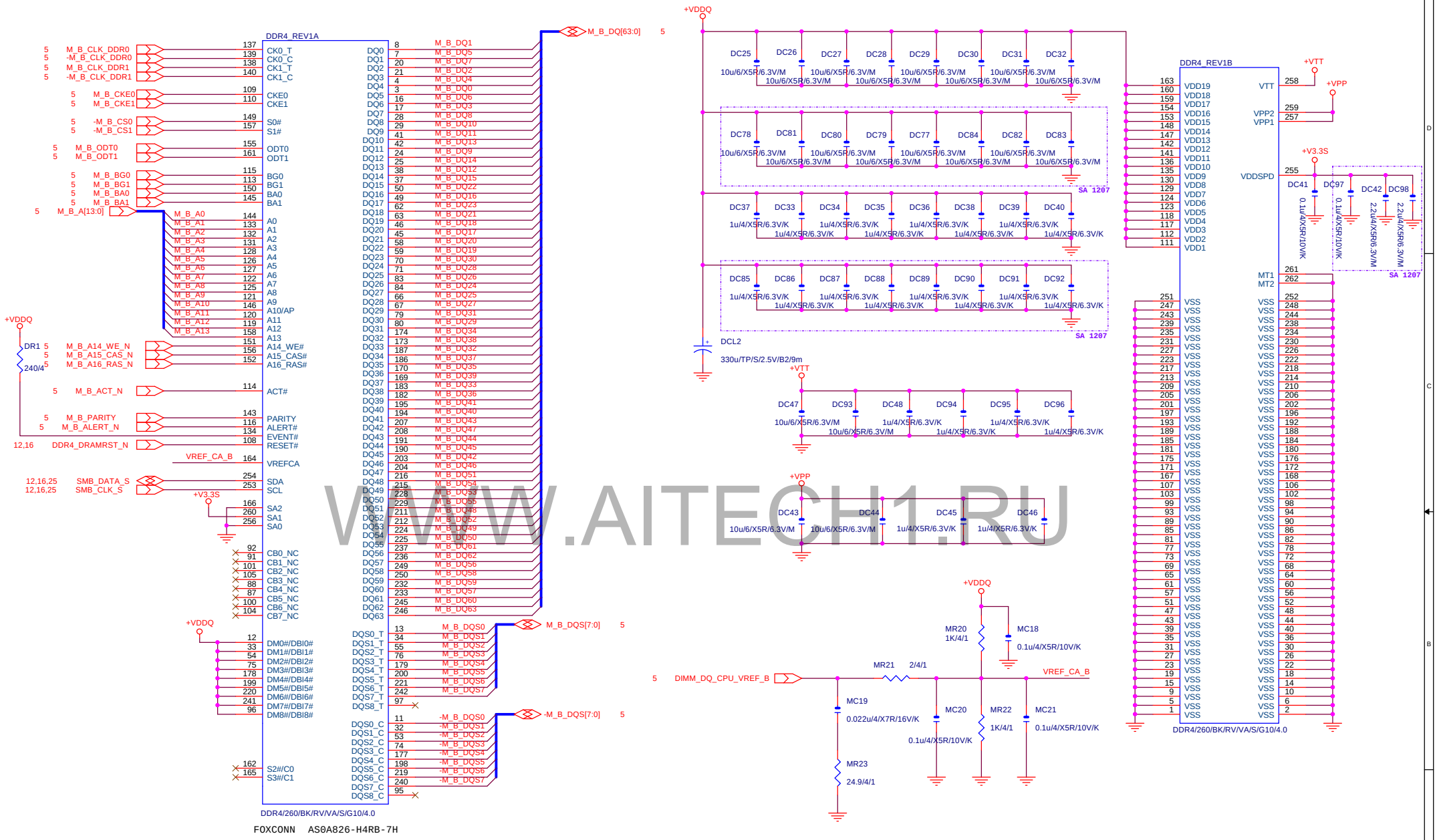
GIGABYTE TECHNOLOGY COPORATION

Title: CPU_8-Decoupling_Cap

Size | Document Number: GA-RP65X8 | Rev: 1.0

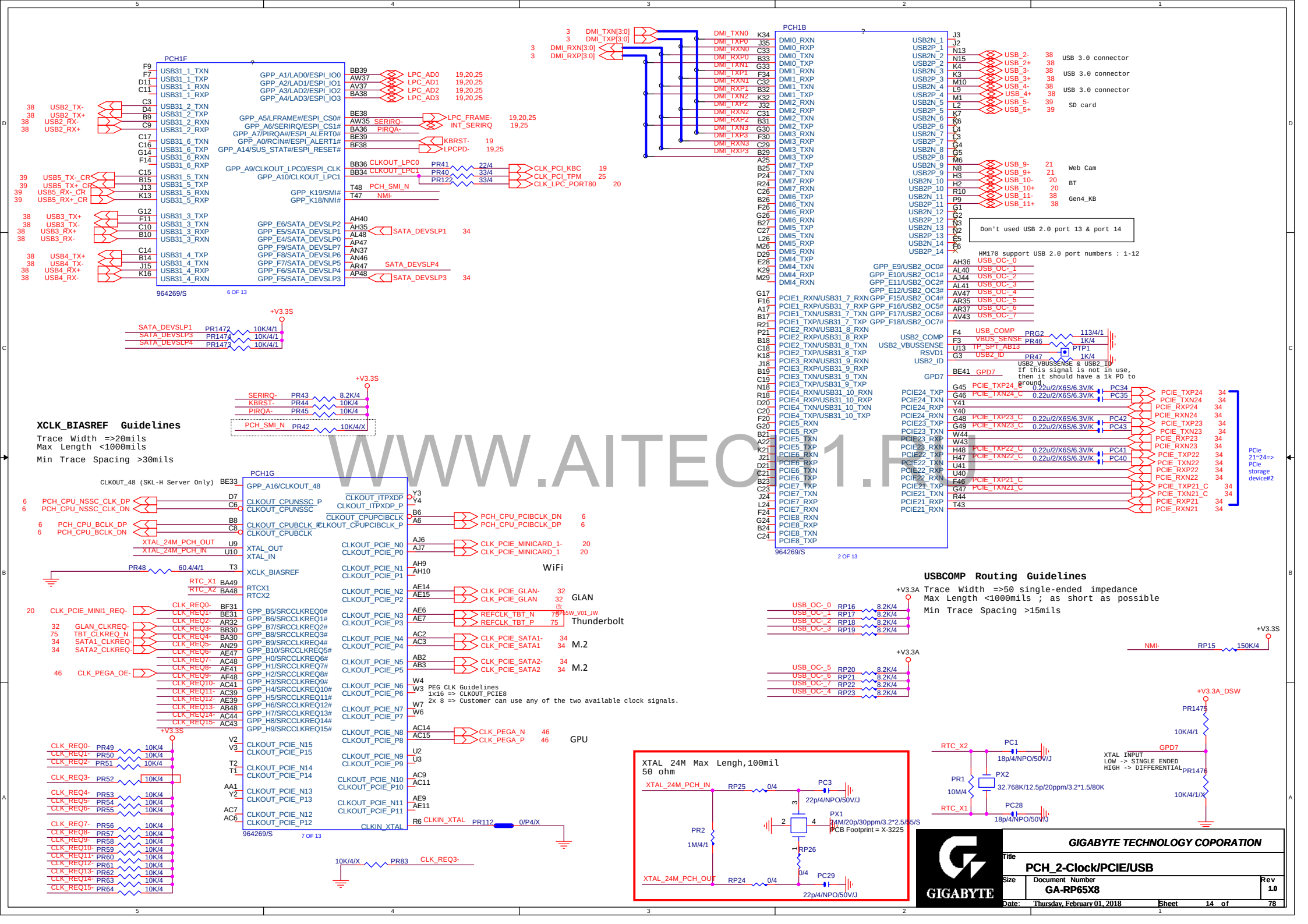
Date: Thursday, February 01, 2018 | Sheet 11 of 78

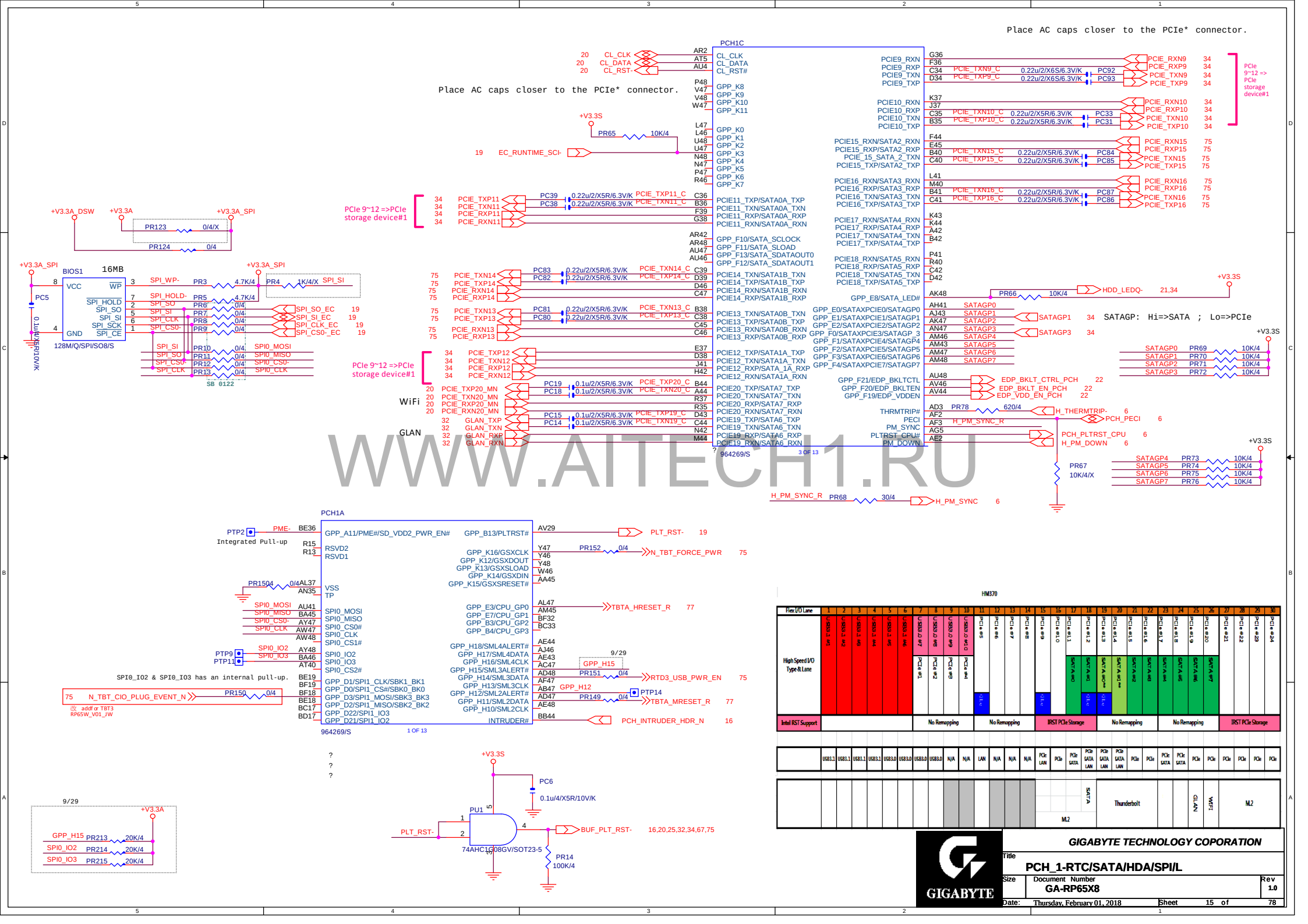




GIGABYTE TECHNOLOGY COPORATION

Title	DDR3L_Channel-B	
Size	Document Number GA-RP65X8	Rev 1.0
Date: Thursday, February 01, 2018	Sheet 13 of 78	





coffee lake Intel review

support Deep Sx state

V02:PR24 NC

SML0ALERT# / GPP_C5
This signal has a weak internal pull-down.
0 = LPC is selected for EC. (Default)
1 = eSPI is selected for EC.

SKL PCH-H has adequate internal bias resistance on JTAG, PREQ#/PRDY# signals to keep the devices in an idle state without the external pull up resistors.

SPKR / GPP_B14 Top Swap Override

Flash Descriptor Security Override

No Reboot on TCO Timer expiration

3.28x80.6/(1.5+80.6)=3.22

V02:VCCRTC voltage reduced to 3.0V nominal and 3.2V max.

Clear ME RTC register

Clear CMOS

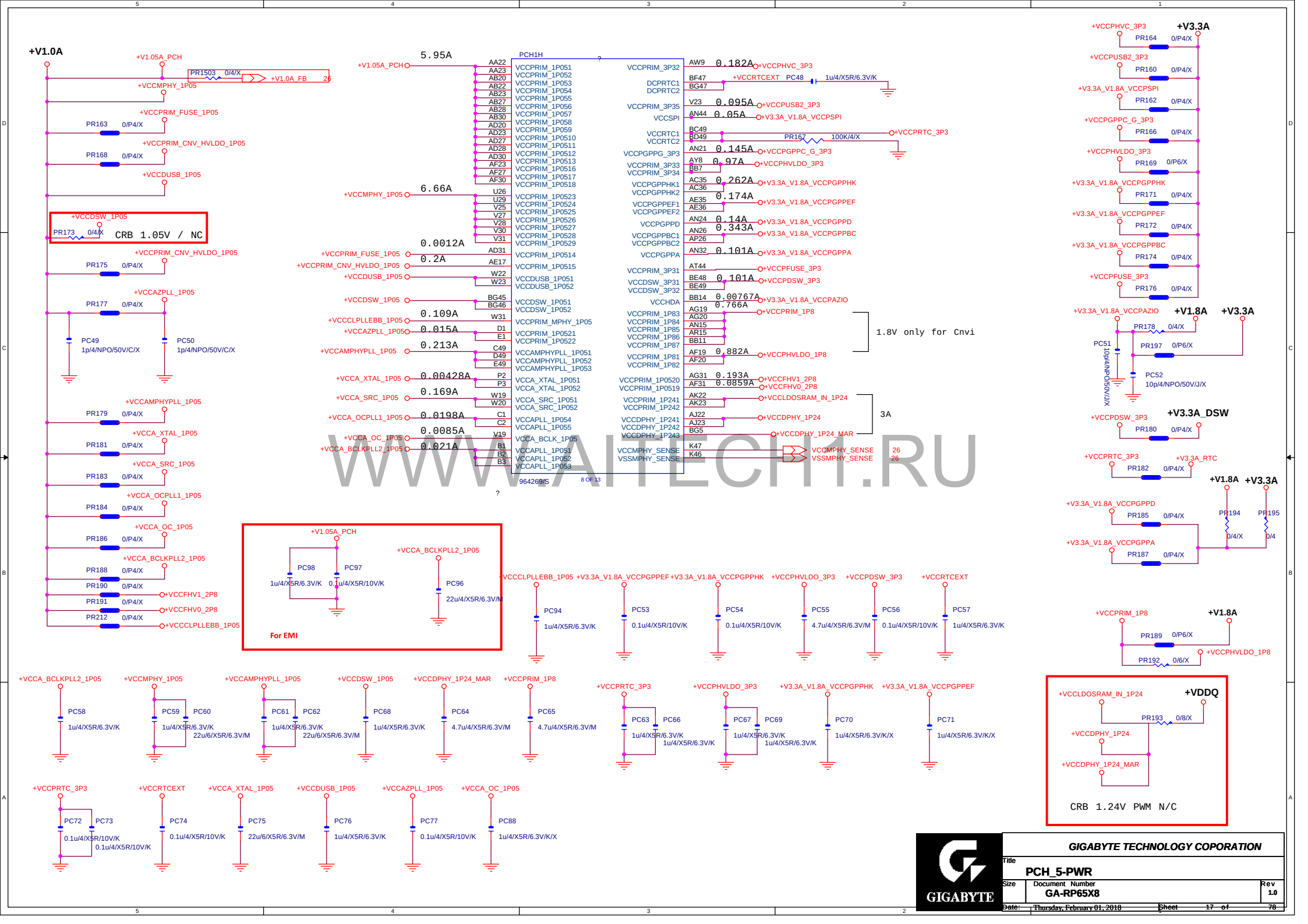
964269/S

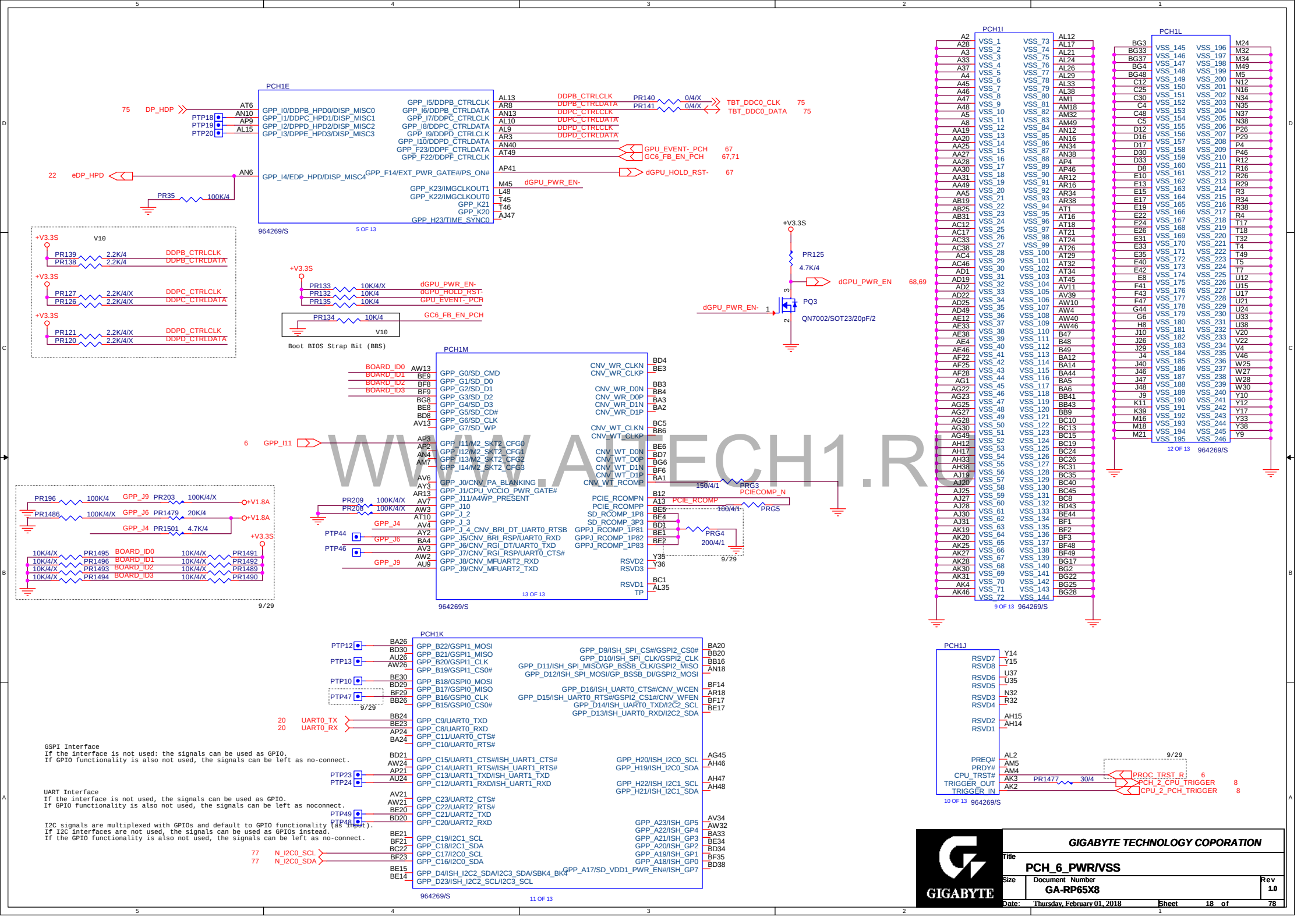
4 OF 13

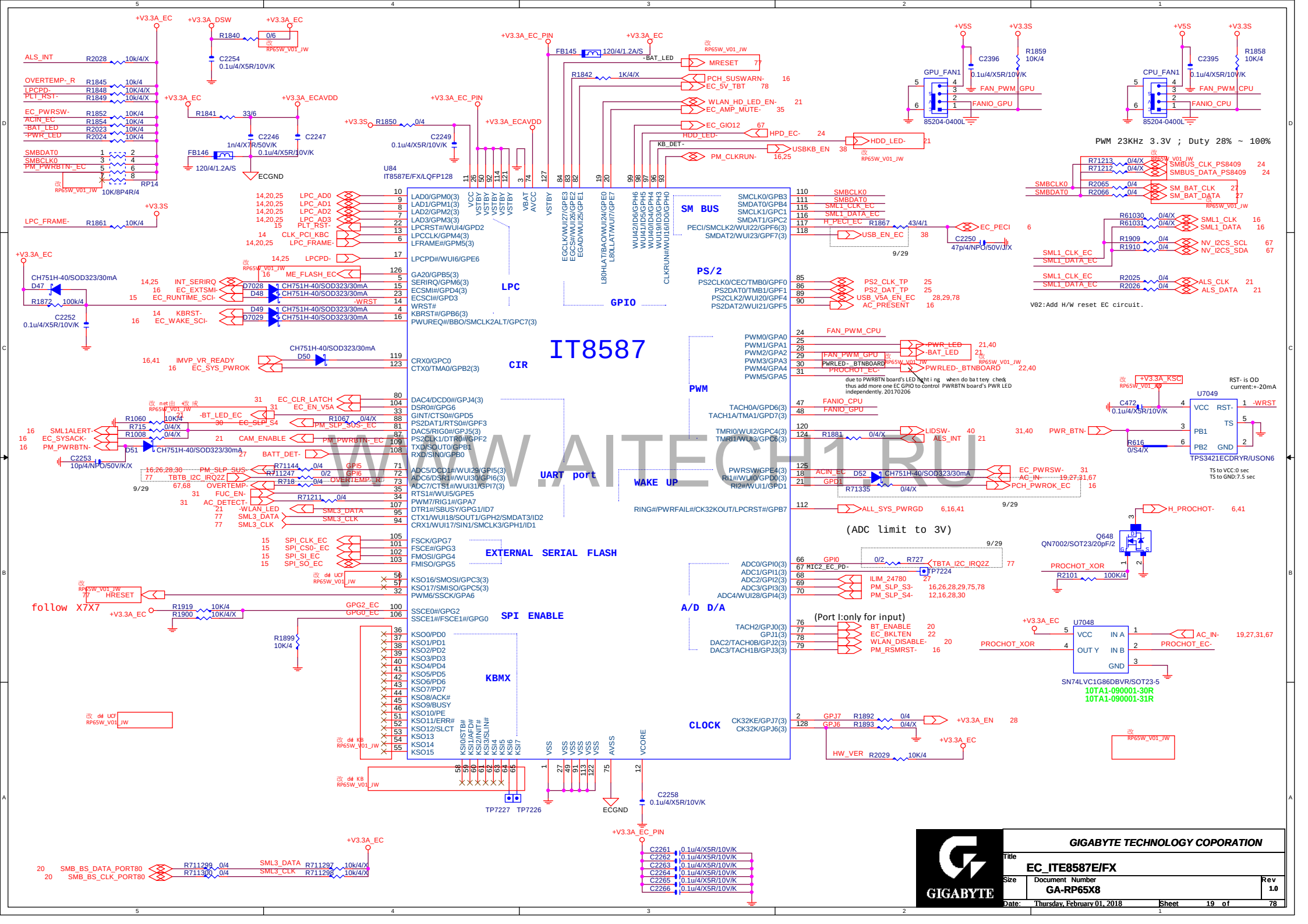
9/29

9/29

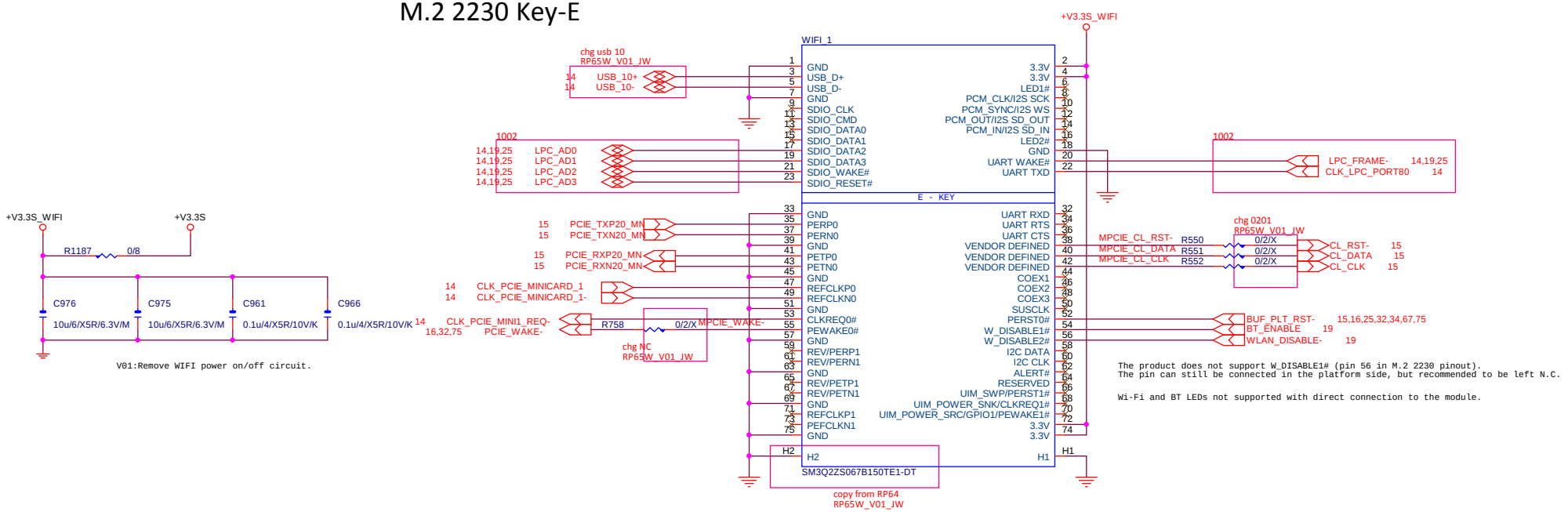
GIGABYTE TECHNOLOGY COPORATION	
Title	PCH_3-DMI/FDI/RGB/PWR-Man
Size	Document Number: GA-RP65X8 — Rev: 1.0
Date: Thursday, February 01, 2018	Sheet 16 of 78



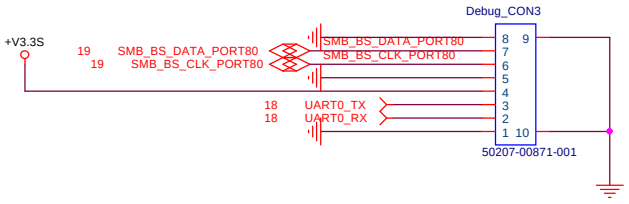




M.2 2230 Key-E



MB Side



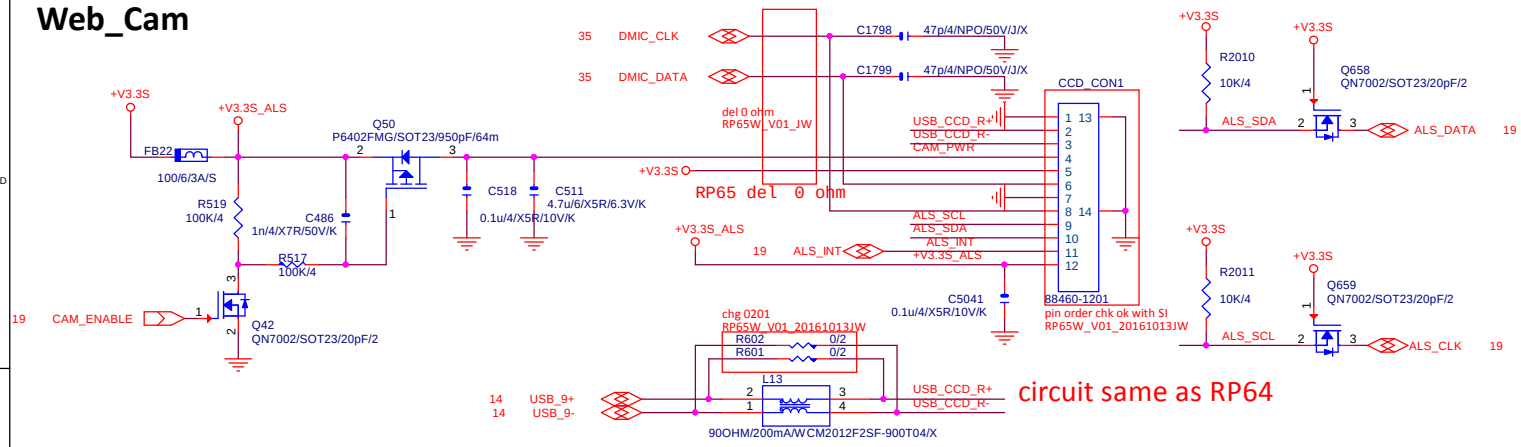
GIGABYTE TECHNOLOGY COPORATION

Title: WiFi

Size	Document Number	Rev
	GA-RP65X8	1.0

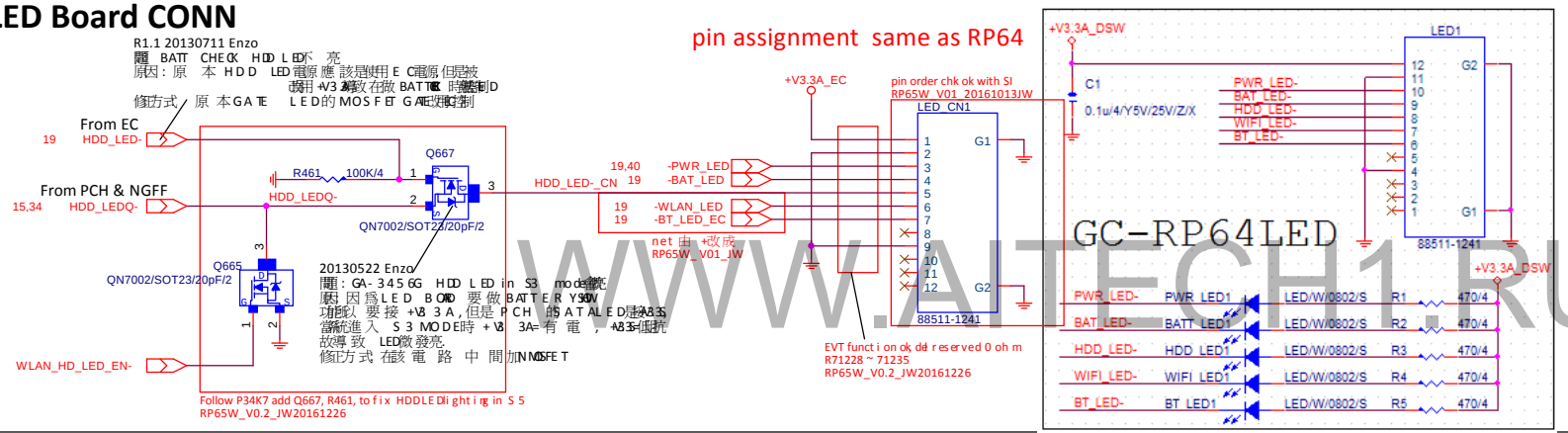
Date: Thursday, February 01, 2018 Sheet 20 of 78

Web_Cam



del gen1 K.B.
RP65W_V01_20160901JW

LED Board CONN

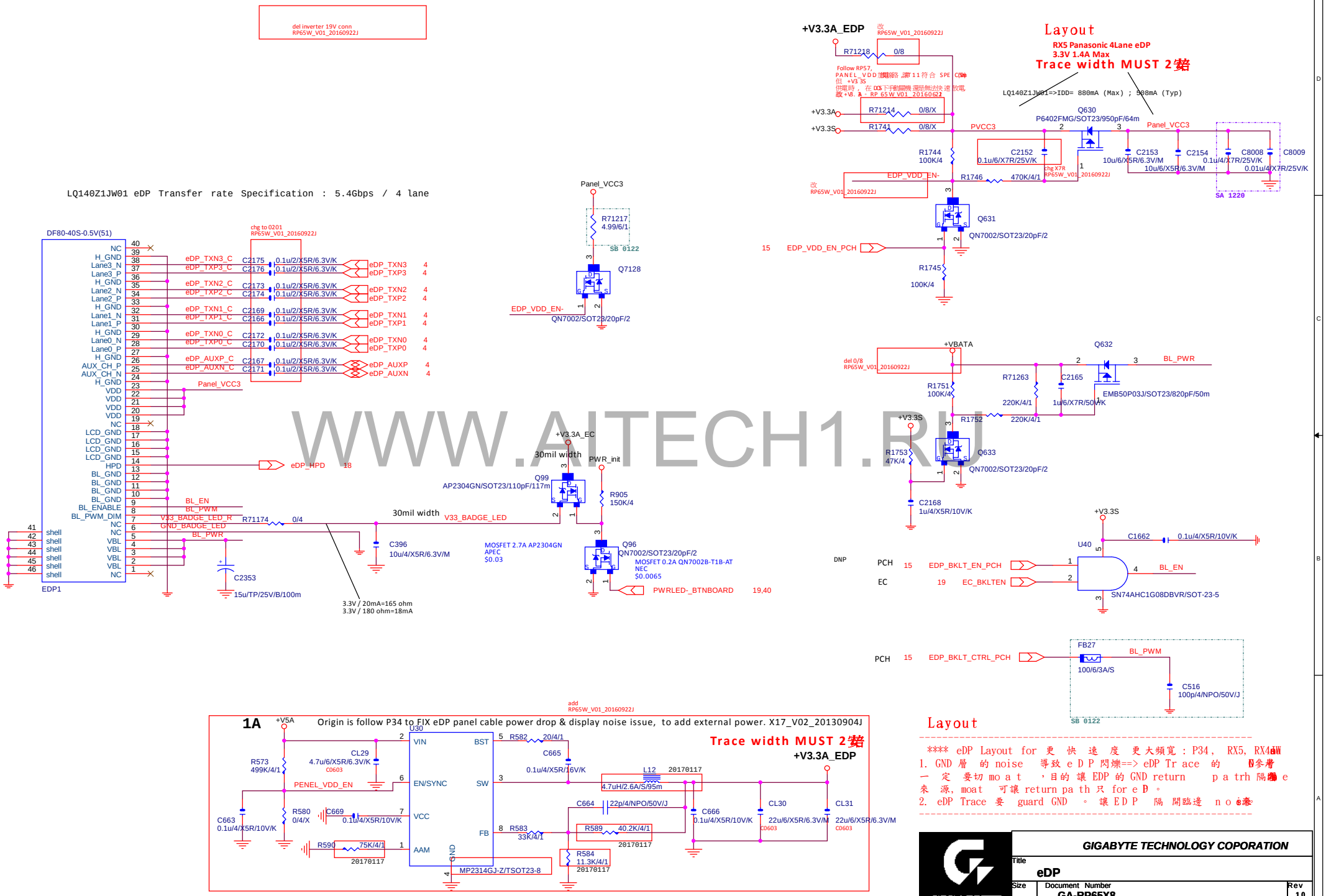


RP65 改
20160901 RP65
del gen1 K.B.

RP65 改
20160901 RP65
del MKBK_CTRL

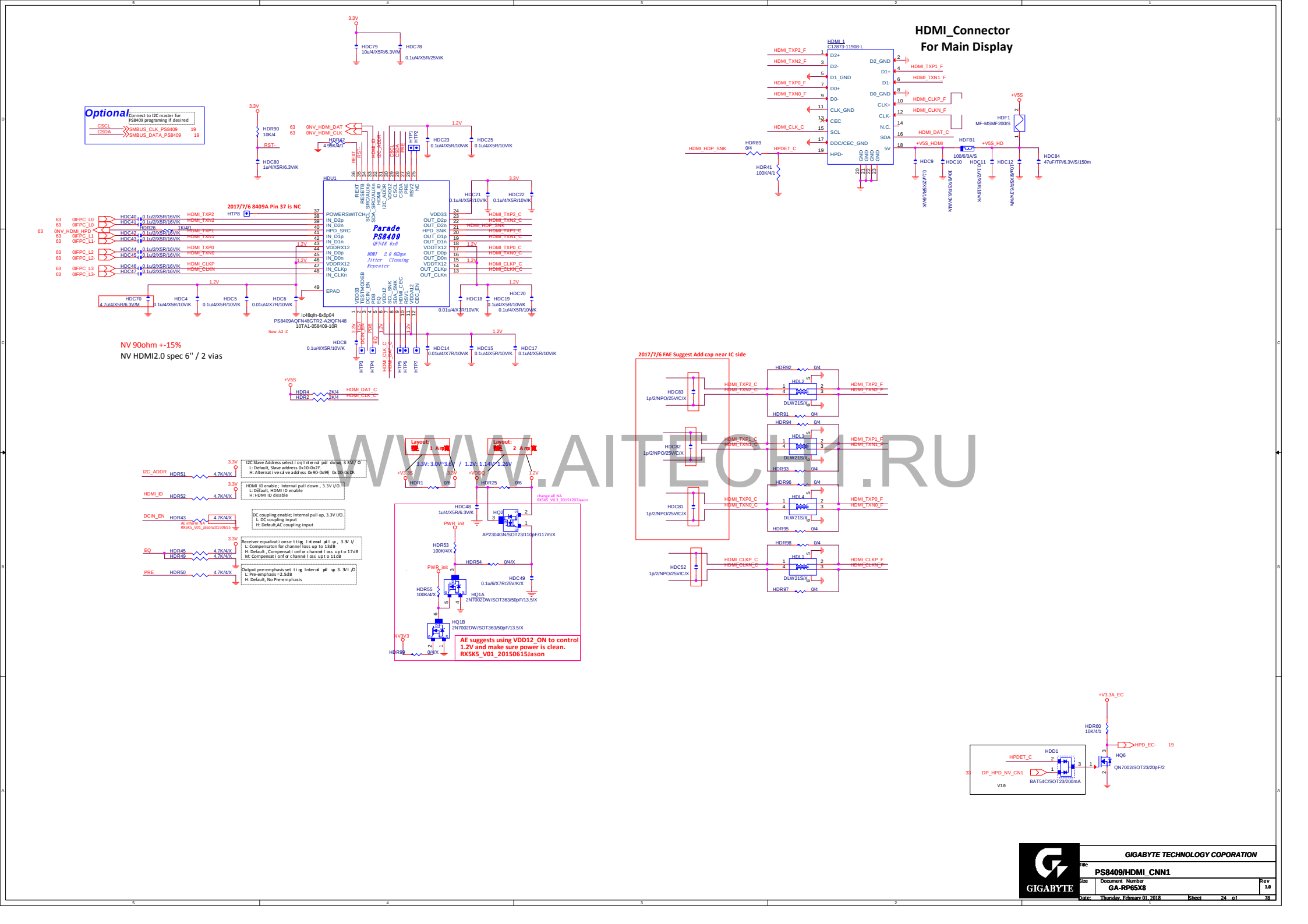
GIGABYTE TECHNOLOGY COPORATION

Title	Board_Connectors	
Size	Document Number GA-RP65X8	Rev 1.0
Date: Thursday, February 01, 2018	Sheet 21 of 78	



GIGABYTE

GIGABYTE TECHNOLOGY COPORATION		
Title: PCH_5-PWR		
Size	Document Number: GA-RP65X8	Rev: 1.0
Date: Thursday, February 01, 2018	Sheet 23 of 78	



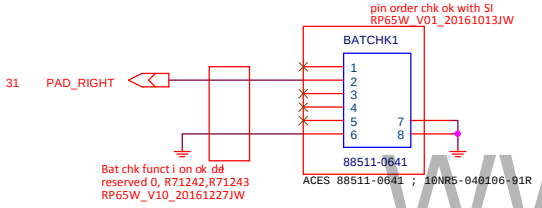
Click Pad

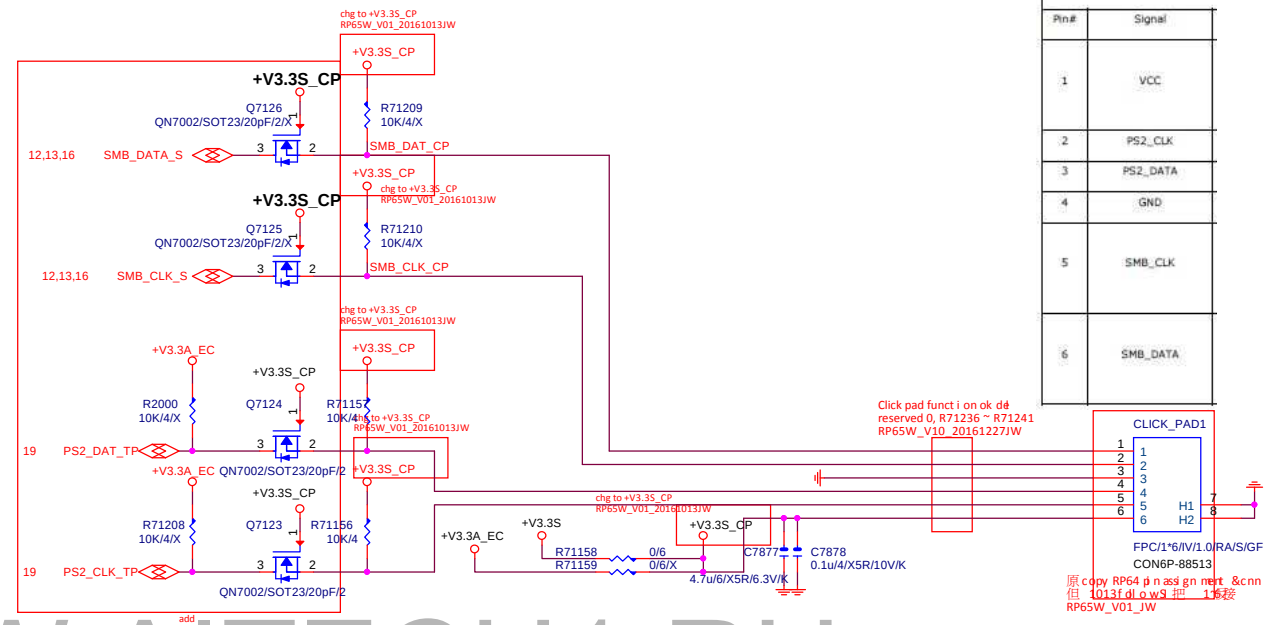
SA469A-32H2 Pin Assignment

Pin#	Signal
1	VCC
2	PS2_CLK
3	PS2_DATA
4	GND
5	SMB_CLK
6	SMB_DATA

Battery_Check_Button for Click_Pad

SI: 受 cable pitch影响只 能用 6pin
FFC 接 接 pin2, pin6
pin2 pin6 時 傳到 NB上 就 是把 pin2 (PAD_RIGHT) 與pin6(GND) 接在
PAD_RIGHT由 floating變 成 GND

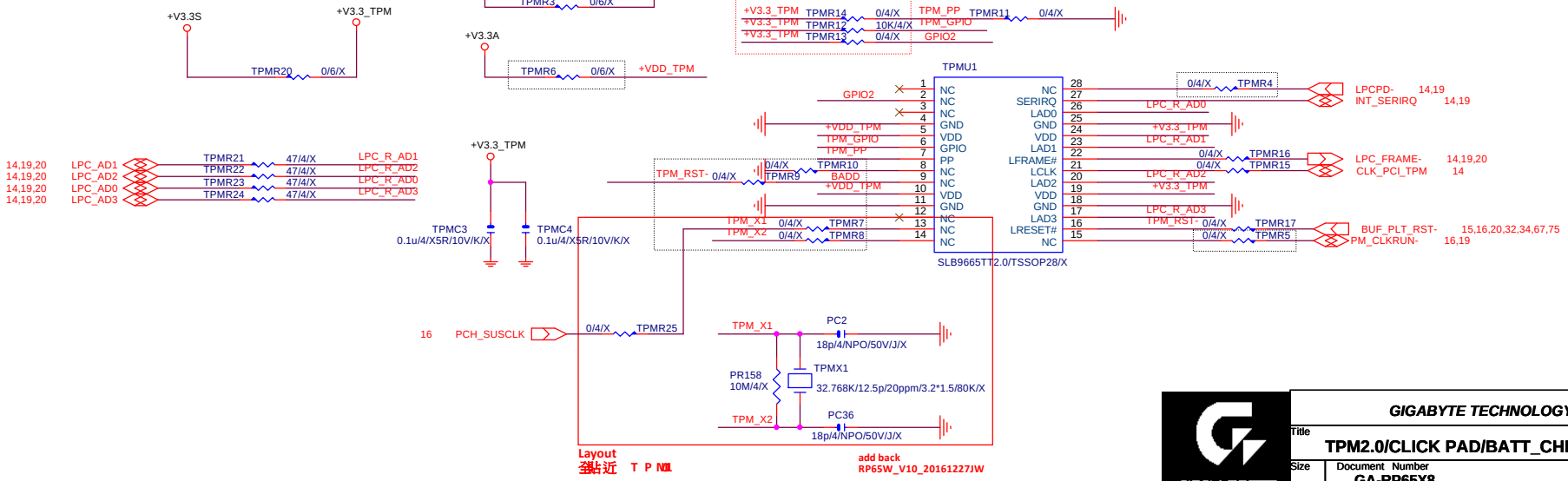




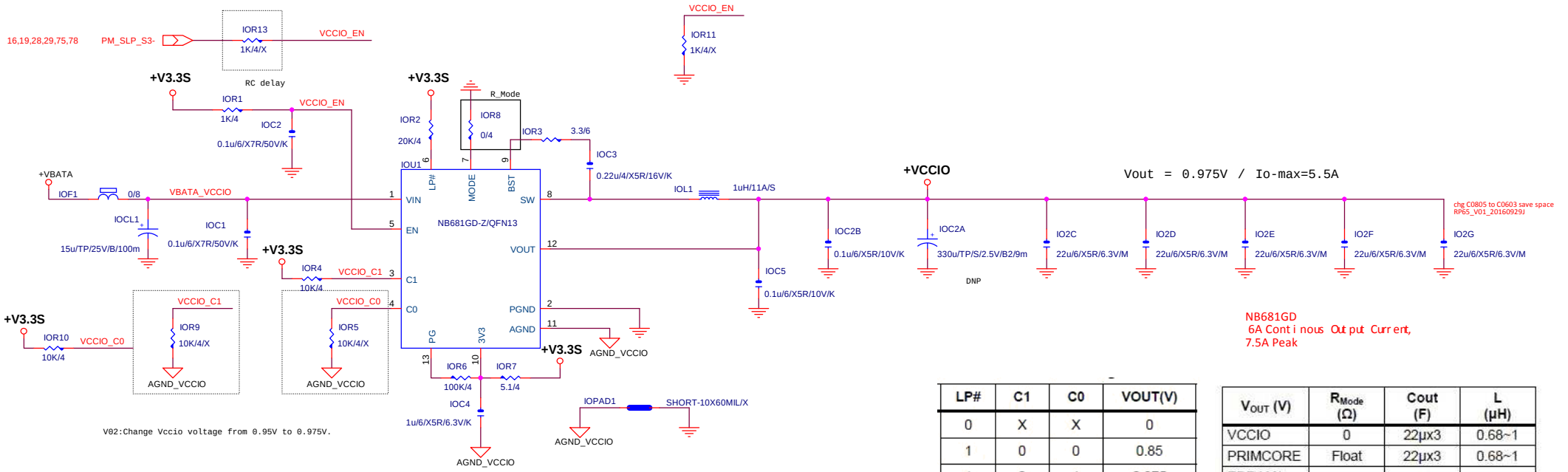
TPM Module

V10:NC

Default TPM9665(co-lay TPM9635)

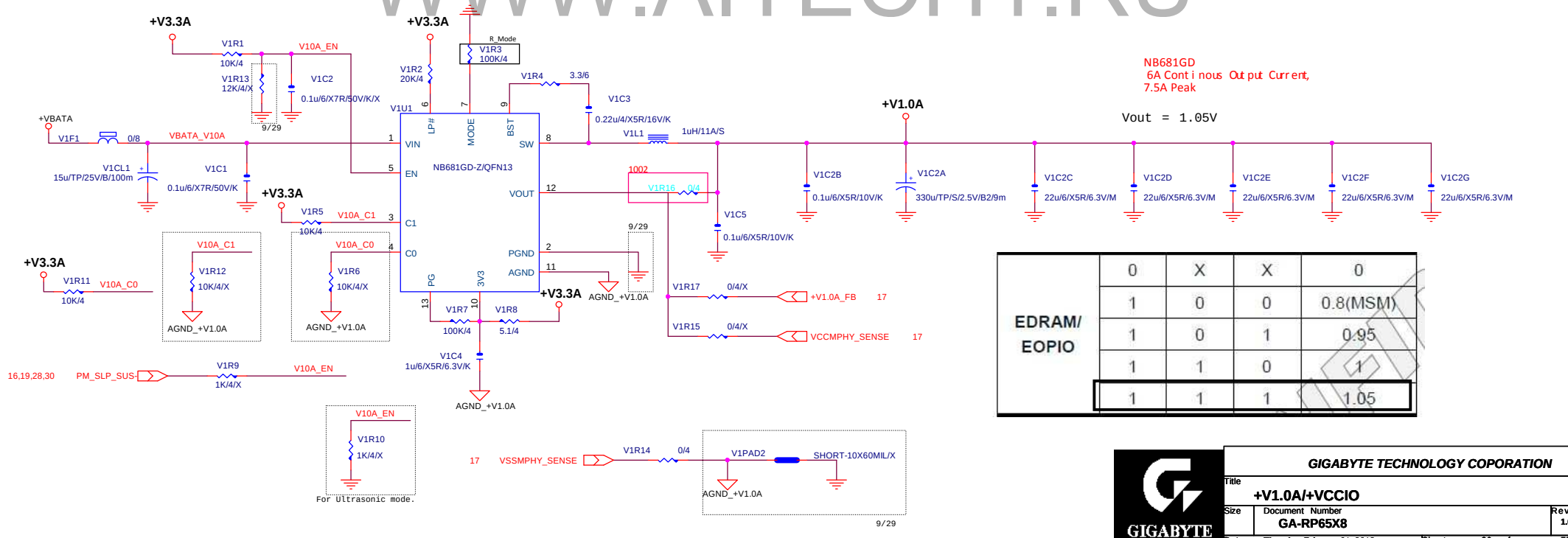


GIGABYTE TECHNOLOGY COPORATION	
Title	TPM2.0/CLICK PAD/BATT_CHECK
Size	Document Number GA-RP65X8 Rev 1.0
Date: Thursday, February 01, 2018	Sheet 25 of 78



LP#	C1	C0	VOUT(V)
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975

V_{OUT} (V)	R_{Mode} (Ω)	Cout (F)	L (μH)
VCCIO	0	22μx3	0.68~1
PRIMCORE	Float	22μx3	0.68~1
EDRAM/ EOPIO/ V1.0A	100K	22μx3	0.68~1
Other	150K	22μx3	0.68~1



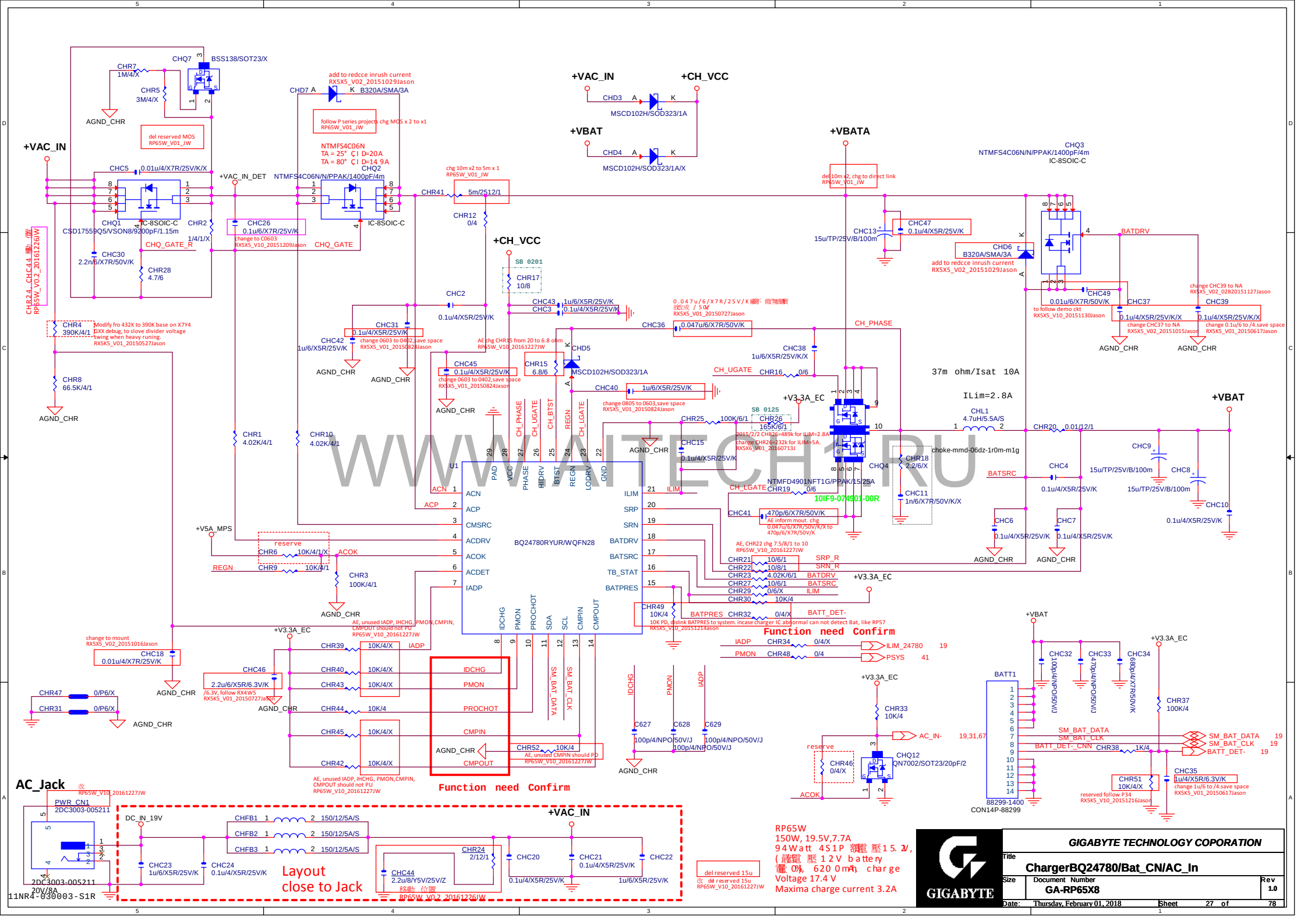
EDRAM/ EOPIO	0	X	X	0
	1	0	0	0.8(MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05

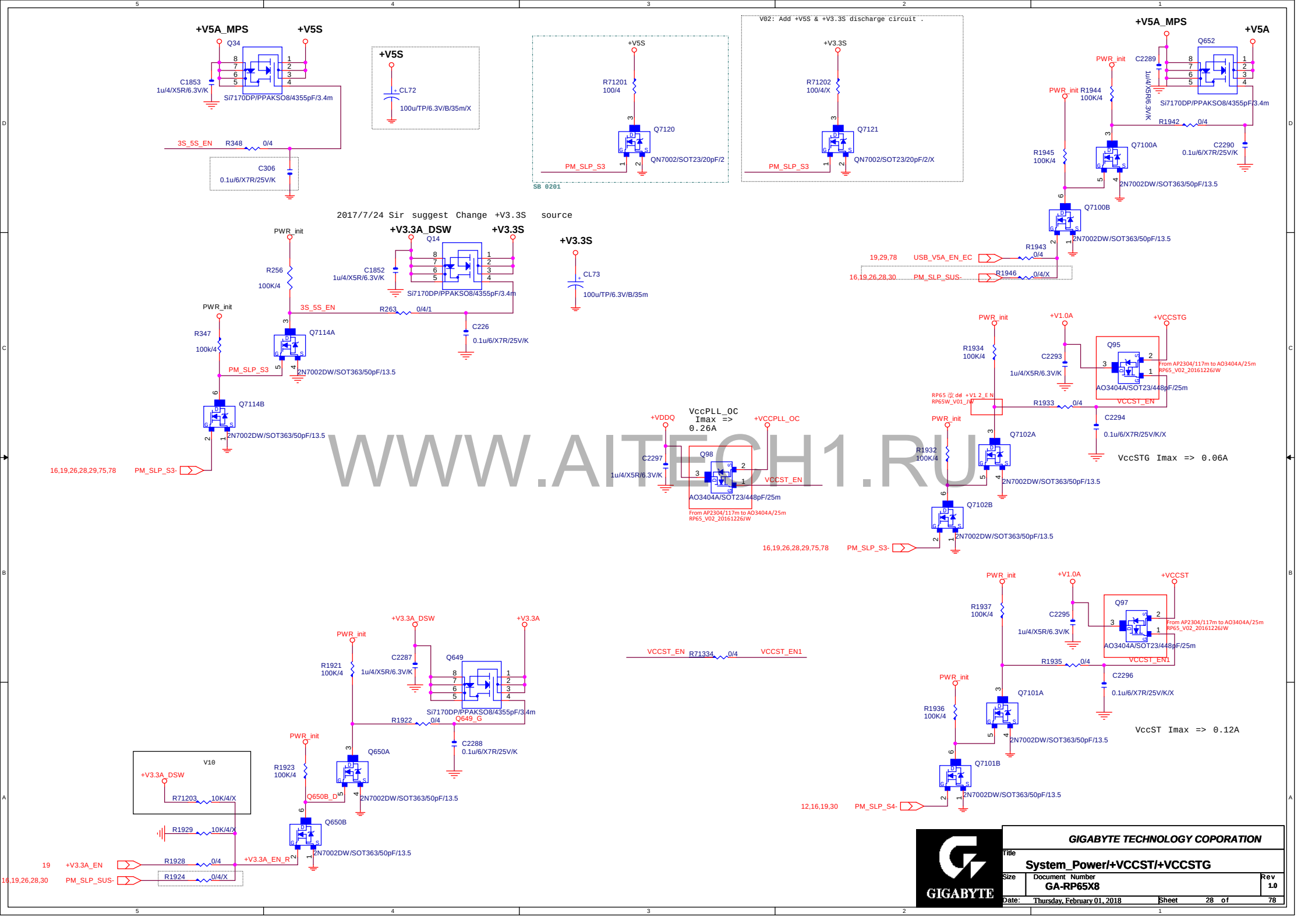
GIGABYTE TECHNOLOGY COPORATION

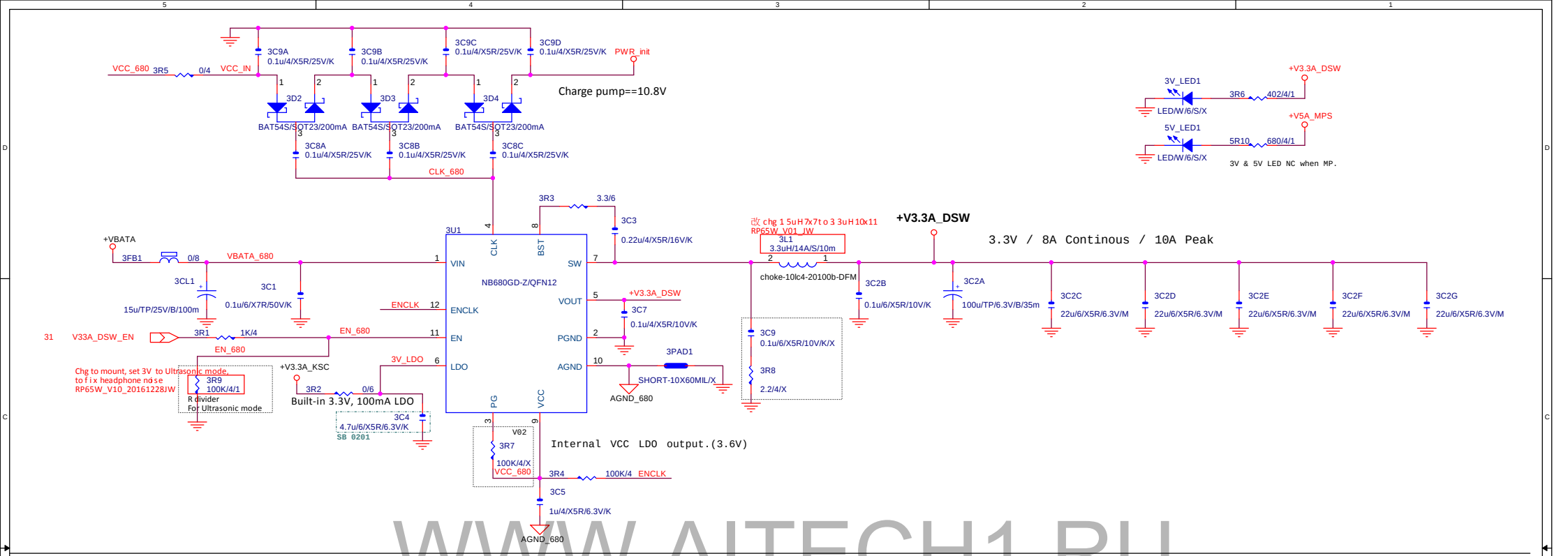
Title: +V1.0A/+VCCIO

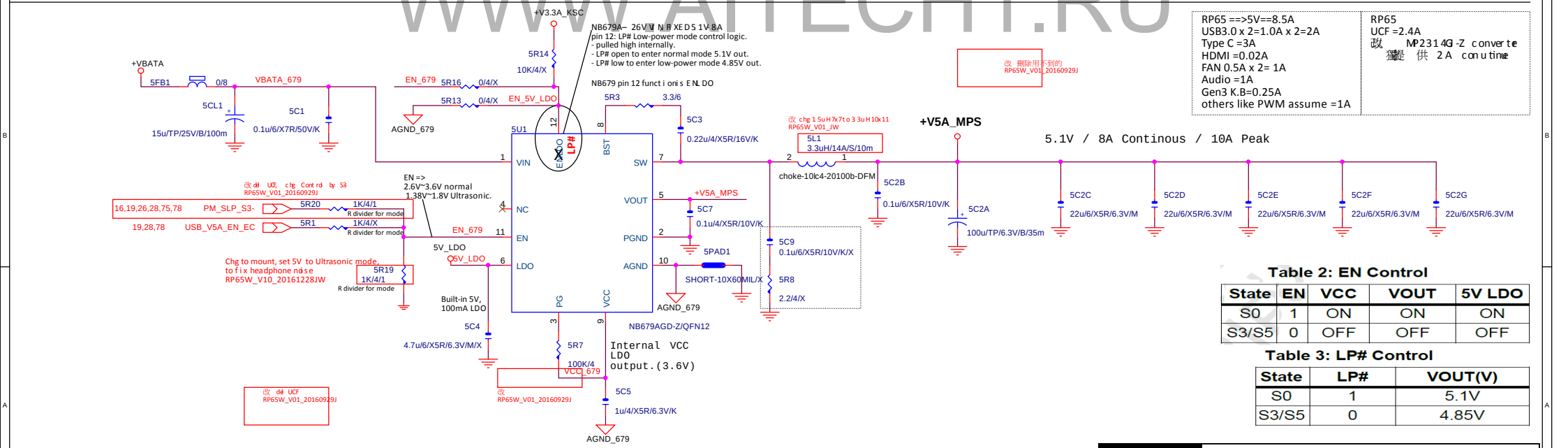
Size: | Document Number: GA-RP65X8 | Rev: 1.0

Date: Thursday, February 01, 2018 | Sheet 26 of 78


+VAC_IN
+CH_VCC
+VBAT
+VBATA
+V3.3A_EC
+V5A_MPS
+VAC_IN_DET
CHQ7 BSS138/SOT23/X
CHR7 1M/4/X
CHR5 3M/4/X
AGND_CHR
CHD7 A K B320A/SMA/3A
add to reddce inrush current RX5X5_V02_20151029Jason
follow P series projects chg MOS x 2 to x1 RP65W_V01_JW
del reserved MOS RP65W_V01_JW
NTMFS4C06N TA = 25° C I D=20A TA = 80° C I D=14.9A
CHQ2 NTMFS4C06N/N/PPAK/1400pF/4m IC-8SOIC-C
CHQ1 IC-8SOIC-C CSD17559Q5/VSON8/9200pF/1.15m
CHC5 0.01u/4/X7R/25V/K/X
CHR2 1/4/1/X
CHC26 0.1u/6/X7R/25V/K change to C0603 RX5X5_V10_20151209Jason
CHQ_GATE_R
CHQ_GATE
CHC30 2.2n/6/X7R/50V/K
CHR28 4.7/6
CHR4 390K/4/1 Modify fro 432K to 390K base on X7Y4 SXX debug, to slove divider voltage swing when heavy runing. RX5K5_V01_20150527Jason
CHR8 66.5K/4/1
CHR1 4.02K/4/1
CHR10 4.02K/4/1
CHR41 5m/2512/1 chg 10m x2 to 5m x 1 RP65W_V01_JW
CHR12 0/4
CHC2 0.1u/4/X5R/25V/K
CHC43 1u/6/X5R/25V/K
CHC3 0.1u/4/X5R/25V/K
CHC36 0.047u/6/X7R/50V/K
CHC31 0.1u/4/X5R/25V/K
CHC42 1u/6/X5R/25V/K change 0603 to 0402,save space RX5X5_V01_20150824Jason
CHC45 0.1u/4/X5R/25V/K change 0603 to 0402,save space RX5X5_V01_20150824Jason
CHR15 6.8/6
CHD5 MSCD102H/SOD323/1A
CHC40 1u/6/X5R/25V/K change 0805 to 0603,save space RX5X5_V01_20150824Jason
AE chg CHR15 from 20 to 6.8 ohm RP65W_V10_20161227JW
CH_PHASE
CH_UGATE
CH_BTST
REGN
CH_LGATE
CHC38 1u/6/X5R/25V/K/X
CHR16 0/6
CHR25 100K/6/1
CHR26 165K/6/1 SB 0125
2015/2/2 CHR26=489k for ILIM=2.8A change CHR26=232k for ILIM=5A. RX5X6_V01_20160713J
CHC15 0.1u/4/X5R/25V/K
CHQ4 NTMFD4901NFT1G/PPAK/15/25A
CHR19 0/6
CHC11 1n/6/X7R/50V/K/X
CHC41 470p/6/X7R/50V/K AE inform mout chg 0.047u/6/X7R/50V/K/X to 470p/6/X7R/50V/K
CHL1 4.7uH/5.5A/S choke-mmd-06dz-1r0m-m1g
CHR20 0.01/12/1
CHC4 0.1u/4/X5R/25V/K
CHC9 15u/TP/25V/B/100m
CHC8 15u/TP/25V/B/100m
CHC10 0.1u/4/X5R/25V/K
CHC6 0.1u/4/X5R/25V/K
CHC7 0.1u/4/X5R/25V/K
CHR18 2.2/6/X
BATSRC
37m ohm/Isat 10A
ILim=2.8A
CHQ3 NTMFS4C06N/N/PPAK/1400pF/4m IC-8SOIC-C
del 10m x2, chg to direct link RP65W_V01_JW
CHC13 15u/TP/25V/B/100m
CHC47 0.1u/4/X5R/25V/K
CHD6 B320A/SMA/3A add to reddce inrush current RX5X5_V02_20151029Jason
BATDRV
CHC49 0.01u/6/X7R/50V/K to follow demo ckt RX5X5_V10_20151130Jason
CHC37 0.1u/4/X5R/25V/K/X change CHC37 to NA RX5X5_V02_20151015Jason
CHC39 0.1u/4/X5R/25V/K/X change CHC39 to NA RX5X5_V02_02B20151127Jason change 0.1u/6 to /4.save space RX5X5_V01_20150617Jason
U1 BQ24780RYUR/WQFN28
ACN ACP CMSRC ACDRV ACOK ACDET IADP
ILIM SRP SRN BATDRV BATSRC TB_STAT BATPRES
IDCHG PMON PROCHOT SDA SCL CMPIN CMPOUT
CHR21 10/6/1 SRP_R
CHR22 10/8/1 SRN_R
CHR23 4.02K/6/1 BATDRV
CHR27 10/6/1 BATSRC
CHR29 0/6/X ILIM
CHR30 10K/4
CHR32 0/4/X BATT_DET-
CHR49 10K/4
10K PD, dslink BATPRES to system. incase charger IC abnormal can not detect Bat, like RP57 RX5X5_V10_20151214ason
Function need Confirm
IADP CHR34 0/4/X ILIM_24780 19
PMOS CHR48 0/4 PSYS 41
CHR39 10K/4/X IADP
CHR40 10K/4/X IDCHG
CHR43 10K/4/X PMON
CHR44 10K/4 PROCHOT
CHR45 10K/4/X CMPIN
CHR42 10K/4/X CMPOUT
CHR52 10K/4 AE, unused CMPIN should PD RP65W_V10_20161227JW
AE, unused IADP, IHCHG, PMON, CMPIN, CMPOUT should not PU RP65W_V10_20161227JW
SM_BAT_DATA SM_BAT_CLK
C627 100p/4/NPO/50V/J
C628 100p/4/NPO/50V/J
C629 100p/4/NPO/50V/J
CHR33 10K/4
CHQ12 QN7002/SOT23/20pF/2
CHR46 0/4/X reserve
AC_IN- 19,31,67
ACOK
BATT1 88299-1400 CON14P-88299
CHC32 100p/4/NPO/50V/J
CHC33 470p/4/NPO/50V/J
CHC34 680p/4/X7R/50V/K
CHR37 100K/4
SM_BAT_DATA 19
SM_BAT_CLK 19
BATT_DET- 19
BATT_DET-_CNN CHR38 1K/4
CHR51 10K/4/X
CHC35 1u/4/X5R/6.3V/K change 1u/6 to /4.save space RX5K5_V01_20150617Jason reserved follow P34 RX5K5_V10_20151216Jason
CHC18 0.01u/4/X7R/25V/K change to mount RX5X5_V02_20151016Jason
CHC46 2.2u/6/X5R/6.3V/K /6.3V, follow RX4WS RX5X5_V01_20150727Jason
CHR47 0/P6/X
CHR31 0/P6/X
AC_Jack
PWR_CN1 2DC3003-005211
2DC3003-005211 20V/8A 11NR4-030003-S1R
DC_IN_19V
CHFB1 CHFB2 CHFB3 150/12/5A/S
CHC23 1u/6/X5R/25V/K
CHC24 0.1u/4/X5R/25V/K
Layout close to Jack
CHR24 2/12/1
CHC44 2.2u/8/Y5V/25V/Z 移動 位置 RP65W_V02_20161226JW
CHC20 0.1u/4/X5R/25V/K
CHC21 0.1u/4/X5R/25V/K
CHC22 1u/6/X5R/25V/K
del reserved 15u 改 del reserved 15u RP65W_V10_20161227JW
RP65W 150W, 19.5V,7.7A 94Watt 4S1P 額電壓15.2V, (讓電壓12V battery 電0%, 620 0mA charge Voltage 17.4 V Maxima charge current 3.2A
GIGABYTE TECHNOLOGY COPORATION
Title ChargerBQ24780/Bat_CN/AC_In
Size Document Number GA-RP65X8 Rev 1.0
Date: Thursday, February 01, 2018 Sheet 27 of 78
WWW.AITECH.RU







RP65 ==>5V==8.5A
USB3.0 x 2=1.0A x 2=2A
Type C =3A
HDMI =0.02A
FAN 0.5A x 2= 1A
Audio =1A
Gen3 K.B=0.25A
others like PWM assume =1A

RP65
UCF =2.4A
改 MP2314GJ-Z converte
猶是 供 2A con u time

Table 2: EN Control

State	EN	VCC	VOUT	5V LDO
S0	1	ON	ON	ON
S3/S5	0	OFF	OFF	OFF

Table 3: LP# Control

State	LP#	VOUT(V)
S0	1	5.1V
S3/S5	0	4.85V

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Title: +V3.3A_DSW/+V5A_MPS

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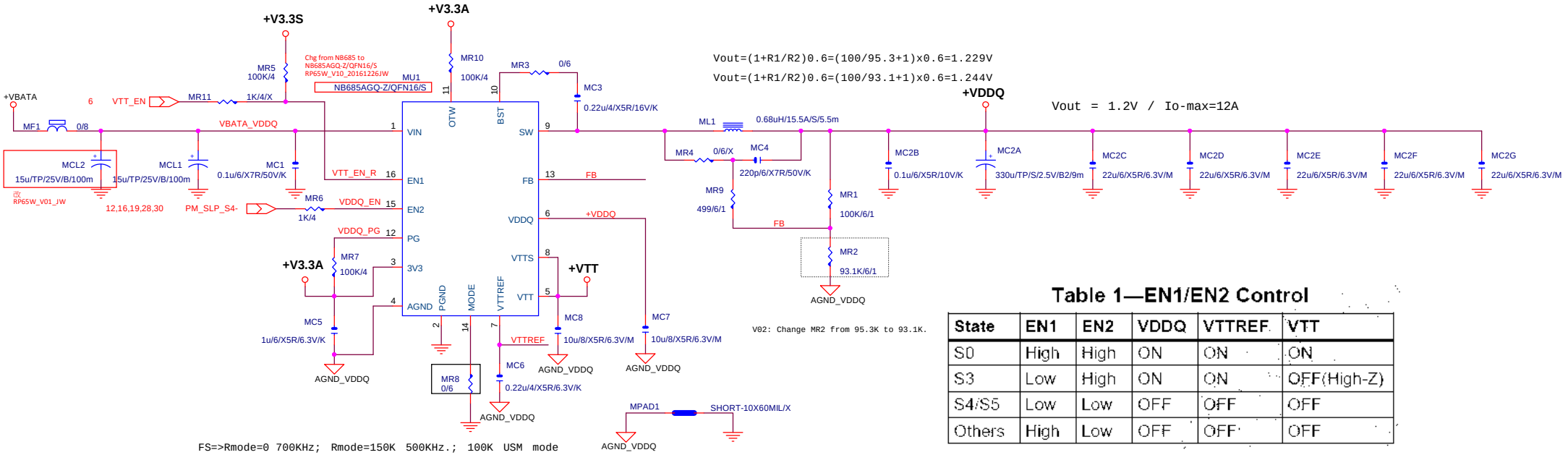


Vout=(1+R1/R2)0.6=(100/95.3+1)x0.6=1.229V

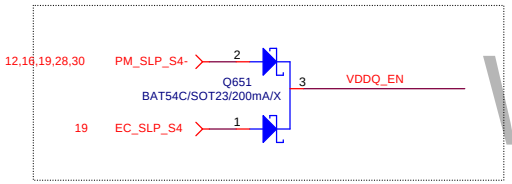
Vout=(1+R1/R2)0.6=(100/93.1+1)x0.6=1.244V

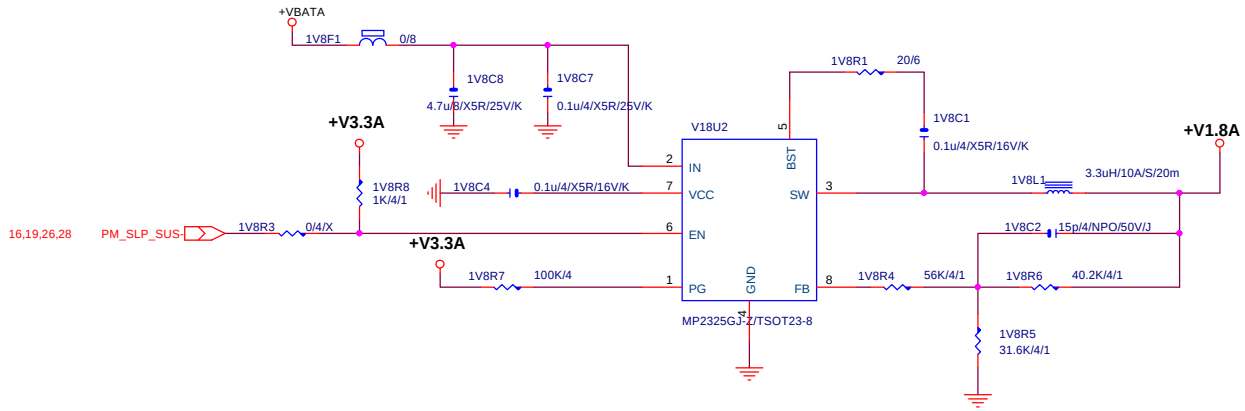
Vout = 1.2V / Io-max=12A

V02: Change MR2 from 95.3K to 93.1K.

Table 1—EN1/EN2 Control

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF





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Title: +VDDQ/+VTT

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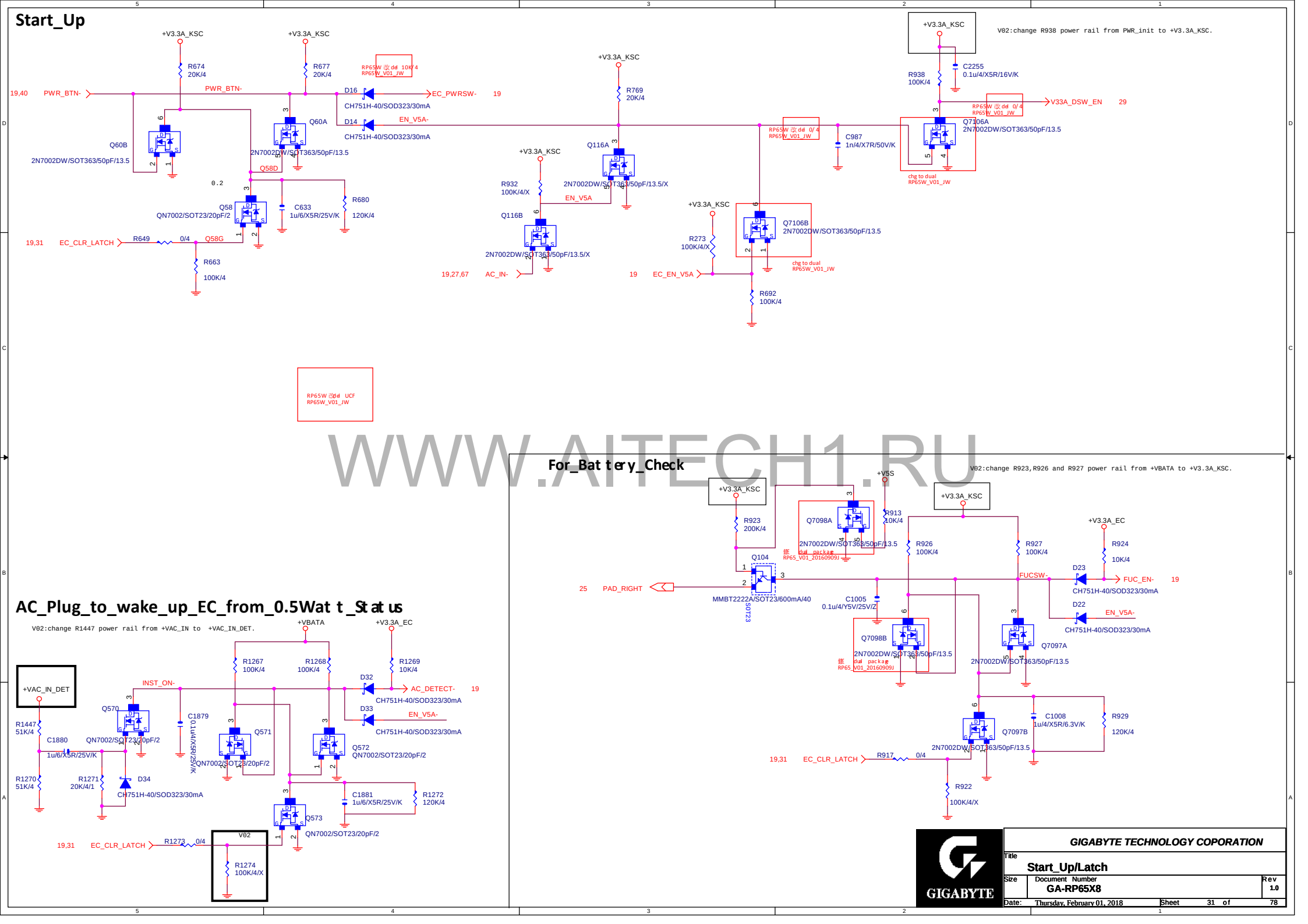

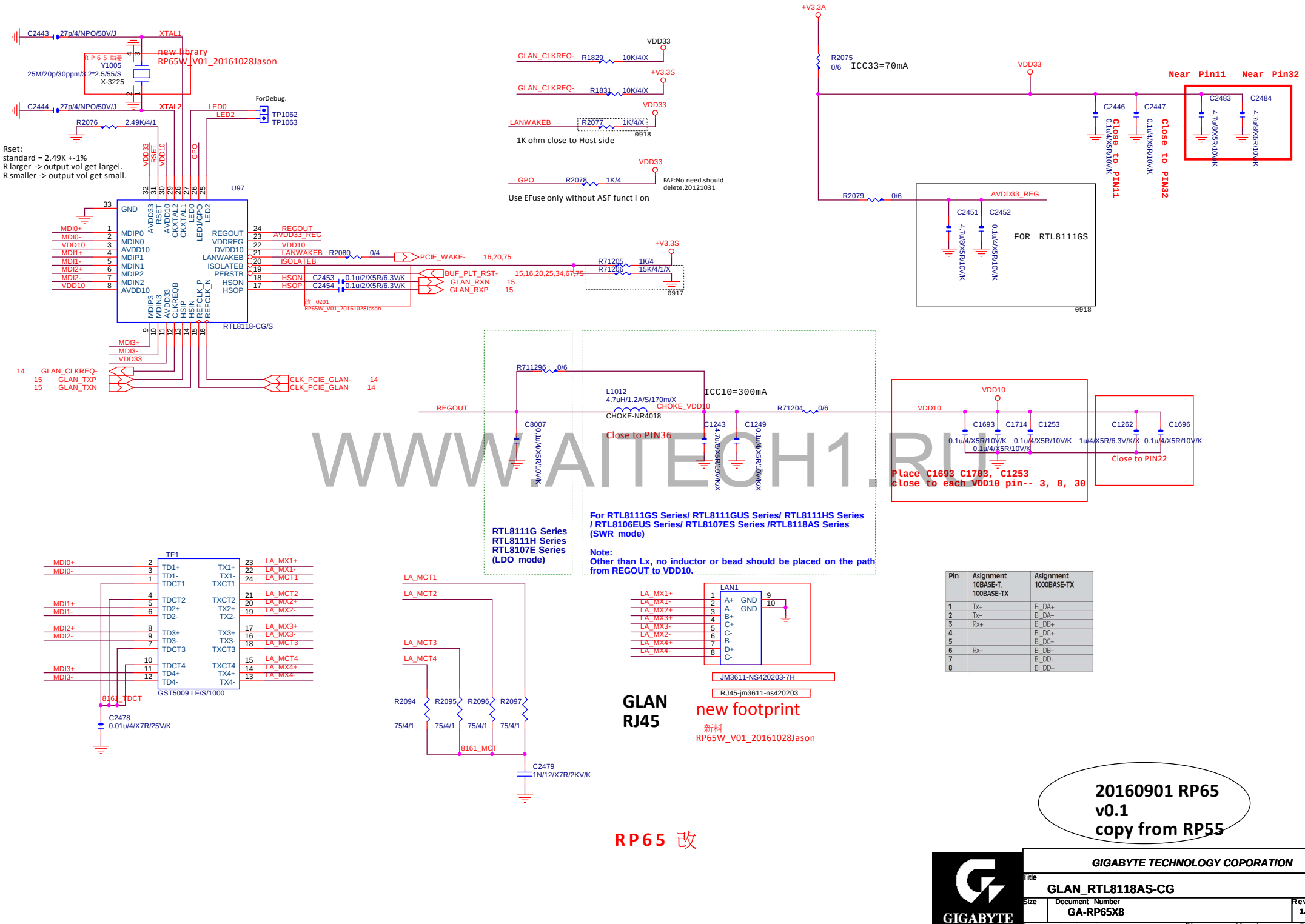

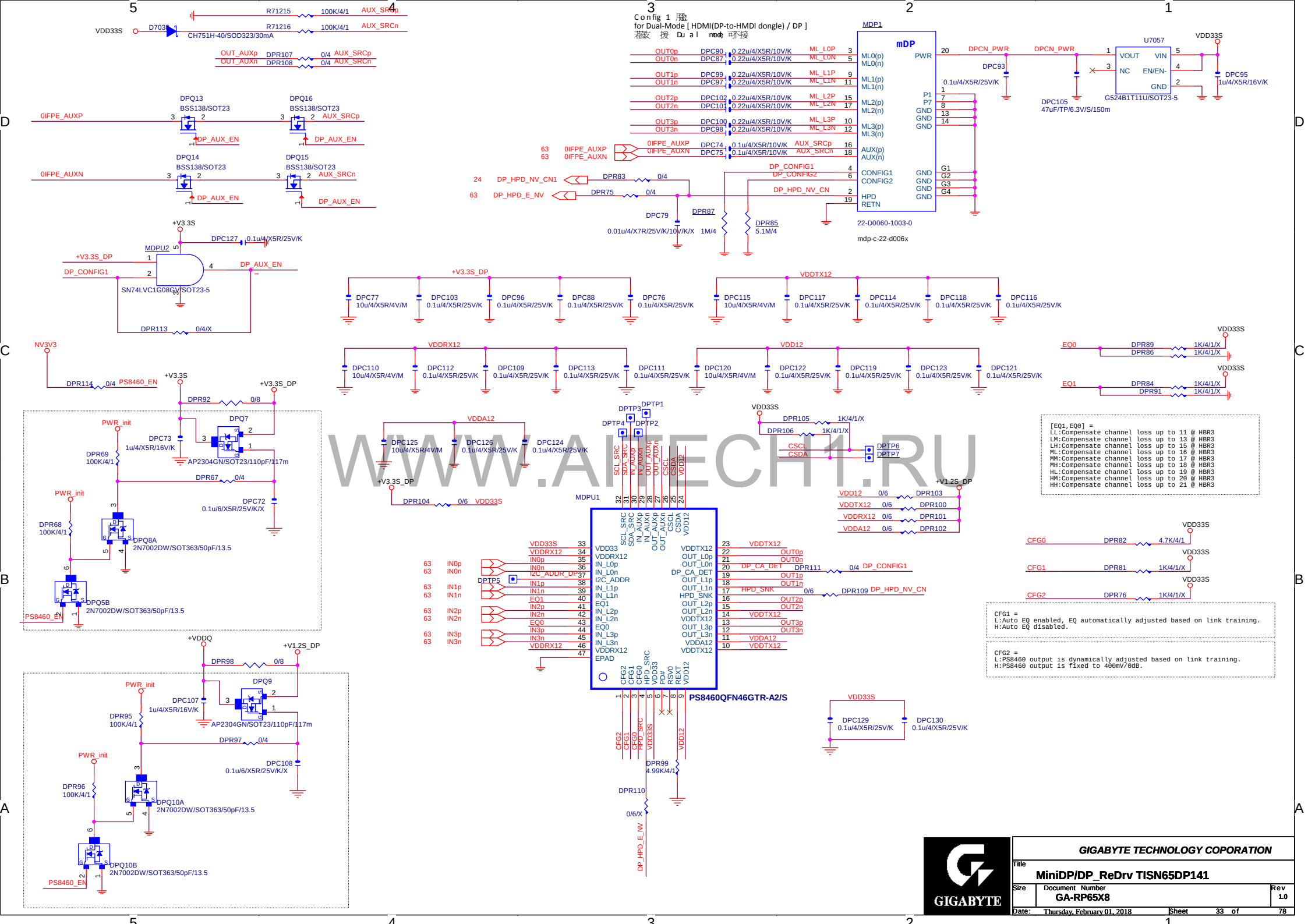

Title	MiniDP/DP_ReDrv TISN65DP141
Size	Document Number: GA-RP65X8 — Rev: 1.0
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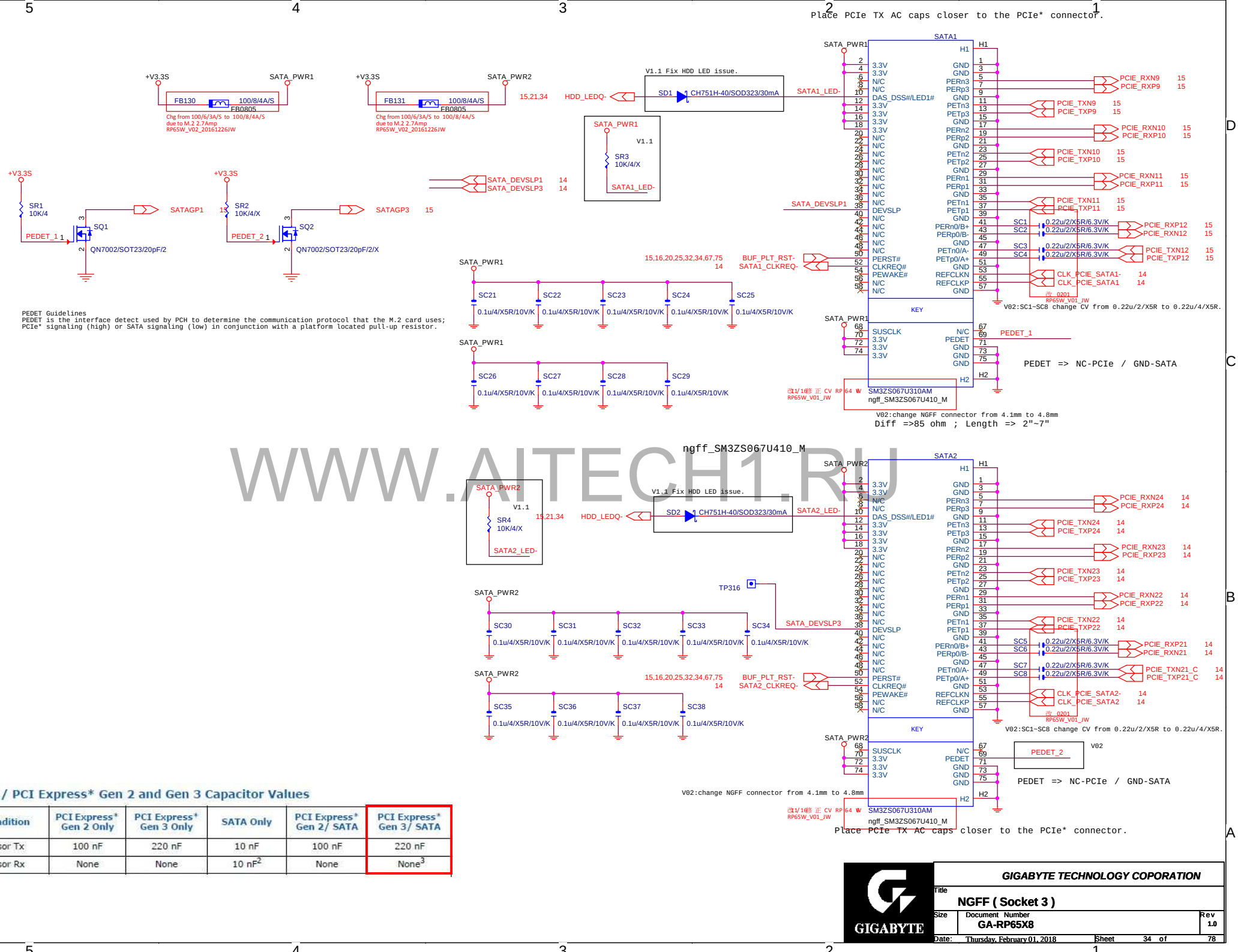
GIGABYTE TECHNOLOGY COPORATION



SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

GIGABYTE	GIGABYTE TECHNOLOGY COPORATION
Title	NGFF (Socket 3)
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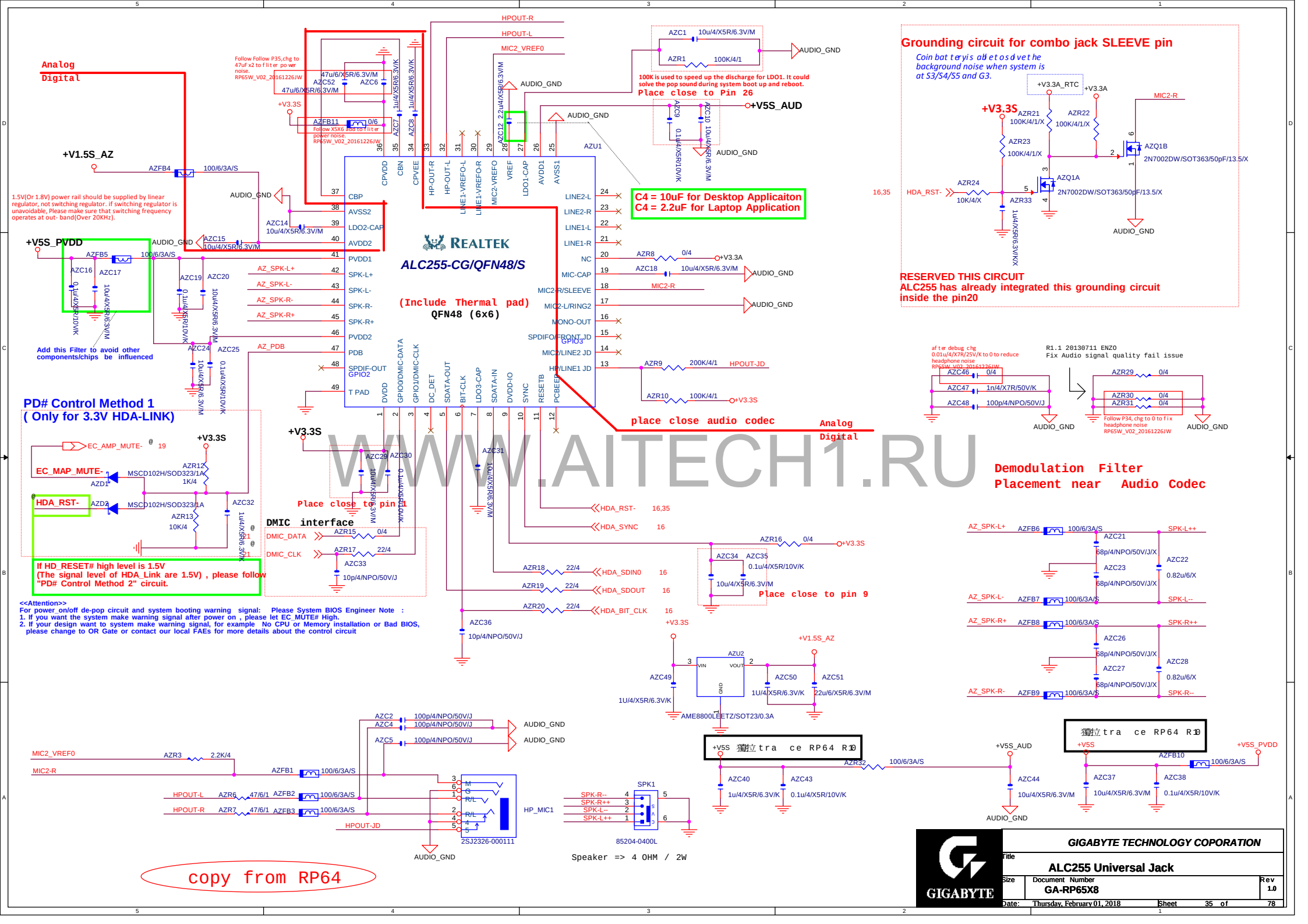

GIGABYTE	GIGABYTE TECHNOLOGY COPORATION	
Title	empty_____	
Size	Document Number GA-RP65X8	Rev 1.0
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GIGABYTE TECHNOLOGY COPORATION		
Title: empty_____		
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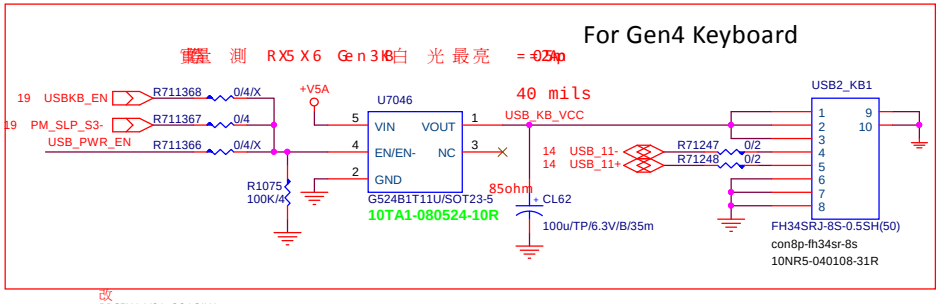
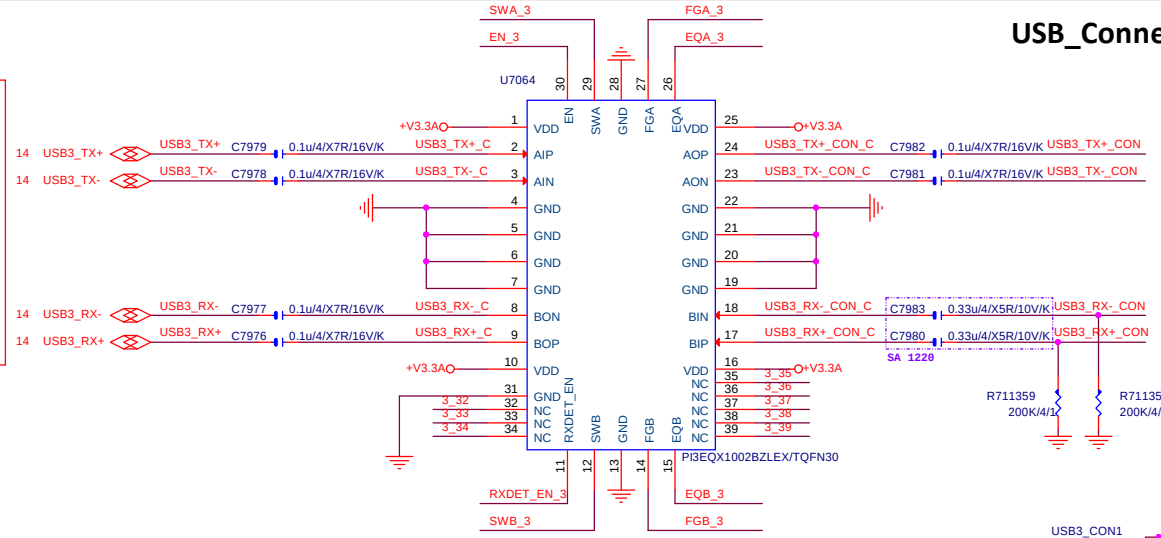
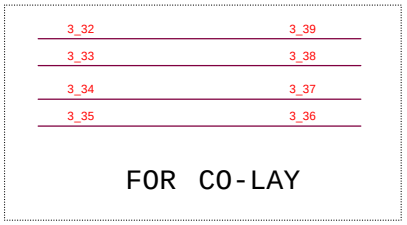
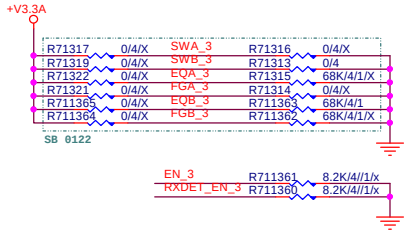
USB_Connector

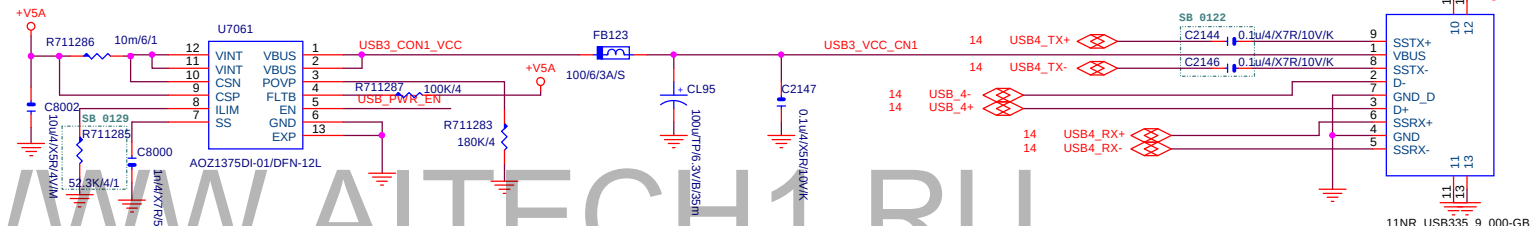


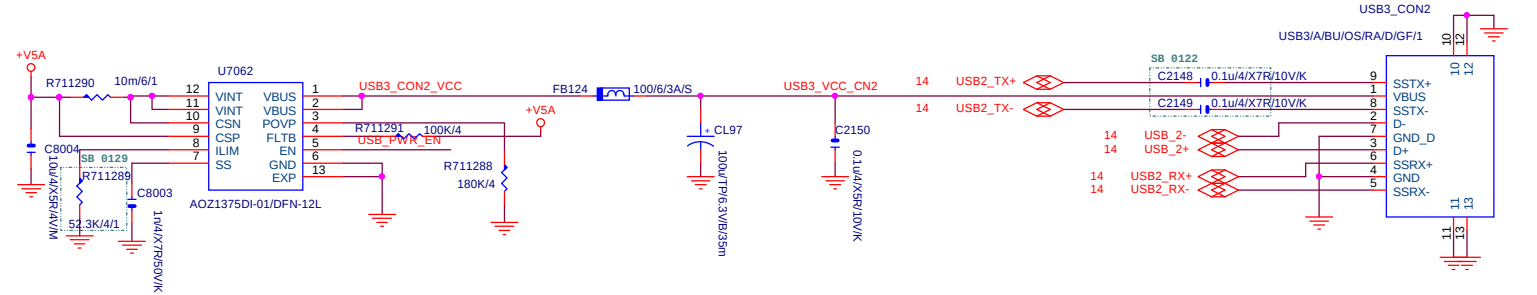
改
RP65W_V01_2016JW

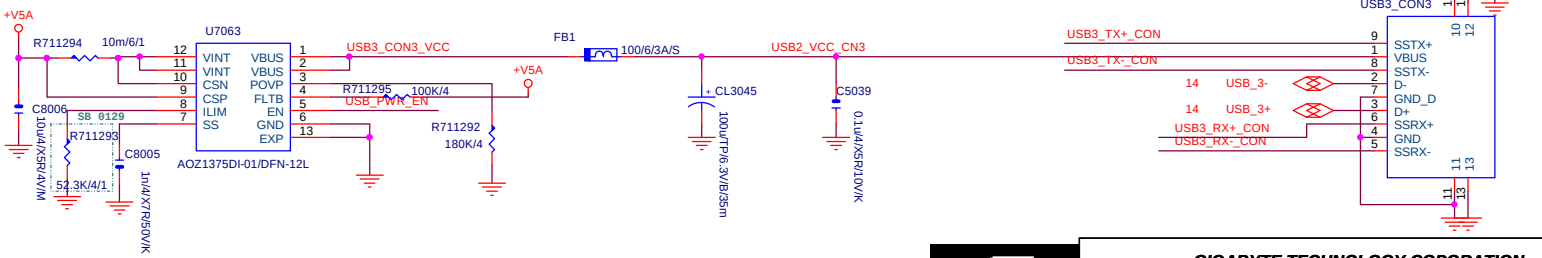


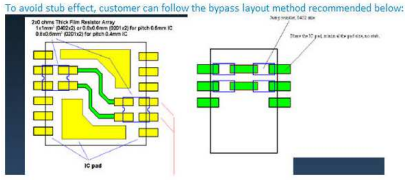












19 USB_EN_EC R1739 0/4 USB_PWR_EN

GIGABYTE TECHNOLOGY COPORATION	
Title	USB3.0x3/Gen4_KB
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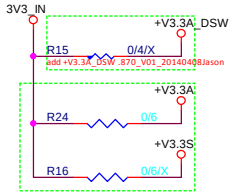
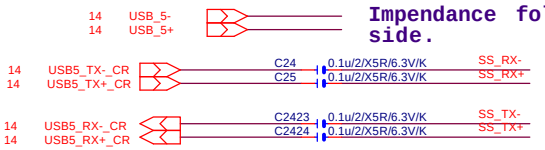
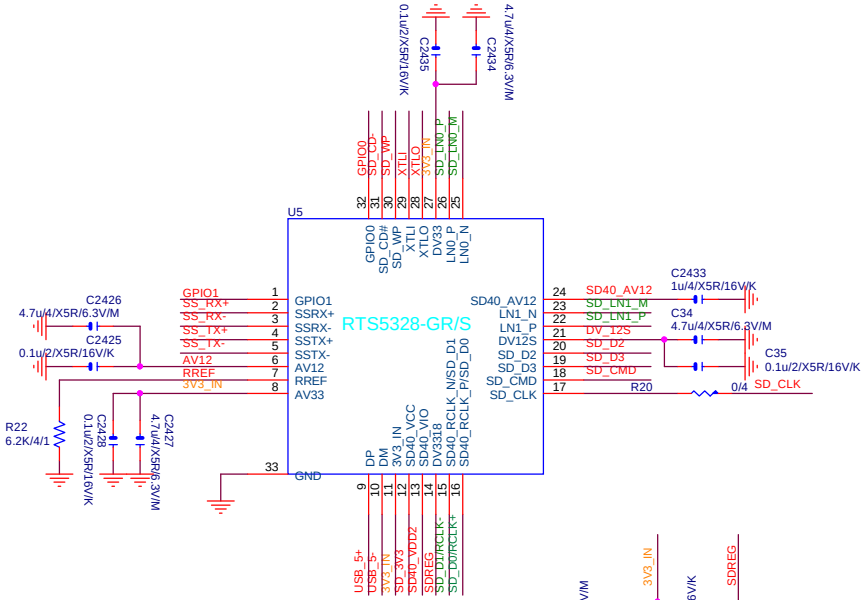
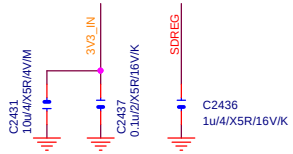
From System's USB3.0 interface

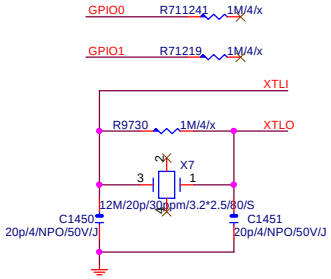


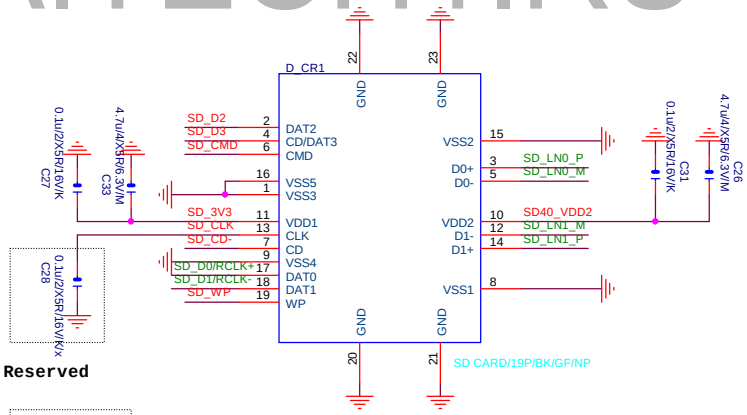


Impendance folllowed as source side.

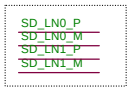








Differentail air 100 ohm



Differentail air 100 ohm

SD UHS-I/UHS-II card socket

GIGABYTE™

Title	Card Reader	
Size A3	Document Number GA-RP65X8	Rev 1.0
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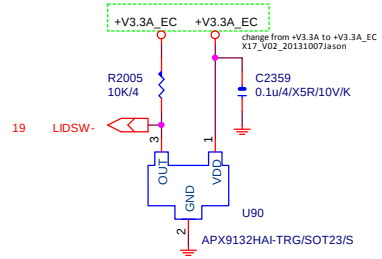
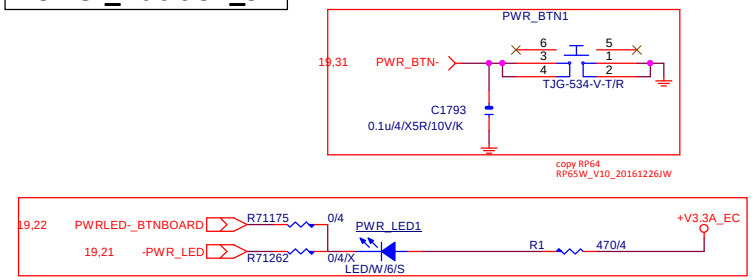
Hall Effect Micro Switch IC



Power_Button_SW



RP65 del touch pad
RP65W_V10_20161226JW

HOLE276_118 x 12

HS5 HOLE236_118/X
HS29 HOLE276_118/X
HS26 HOLE276_118/X
HS6 HOLE276_118/X
HS24 HOLE276_118/X
HS8 HOLE276_118/X
HS31 HOLE260_118/X
HS30 HOLE276_118/X
HS4 HOLE276_118/X
HS2 HOLE276_118/X
HS27 HOLE276_118/X
HS7 HOLE276_118/X

For M.2
M2.0 x H1.2mm stand of f
HS33
STD/INSIDE/D4H1.2M2
HOLE197_138TD

GPU
M2.0 x H1.2mm stand of f
HS43
STD/INSIDE/D4H1.2M2
HOLE197_138TD
HS44
STD/INSIDE/D4H1.2M2
HOLE197_138TD
HS45
STD/INSIDE/D4H1.2M2
HOLE197_138TD
HS46
STD/INSIDE/D4H1.2M2
HOLE197_138TD

For FAN
HS22
STD/INSIDE/D4H1.2M2
HOLE197_138TD
HS23
STD/INSIDE/D4H1.2M2
HOLE197_138TD
follow M.E. Chg from 1.0 to 1.2
RP65W_V10_20161226JW

For CPU
M2.0 x H1.2mm stand of f
HS37
STD/INSIDE/D4H1.2M2
HOLE197_138TD
follow M.E. Chg from 3.0 to 1.2
RP65W_V02_20161226JW
HS38
STD/INSIDE/D4H1.2M2
HOLE197_138TD
HS39
STD/INSIDE/D4H1.2M2
HOLE197_138TD
follow M.E. Chg from 3.0 to 1.2
RP65W_V02_20161226JW

PCB

PCB1
10PMRP65W-TX-S01L

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Title: Lid/PWRBTN/ScrewHole

Size | Document Number: GA-RP65X8 | Rev: 1.0

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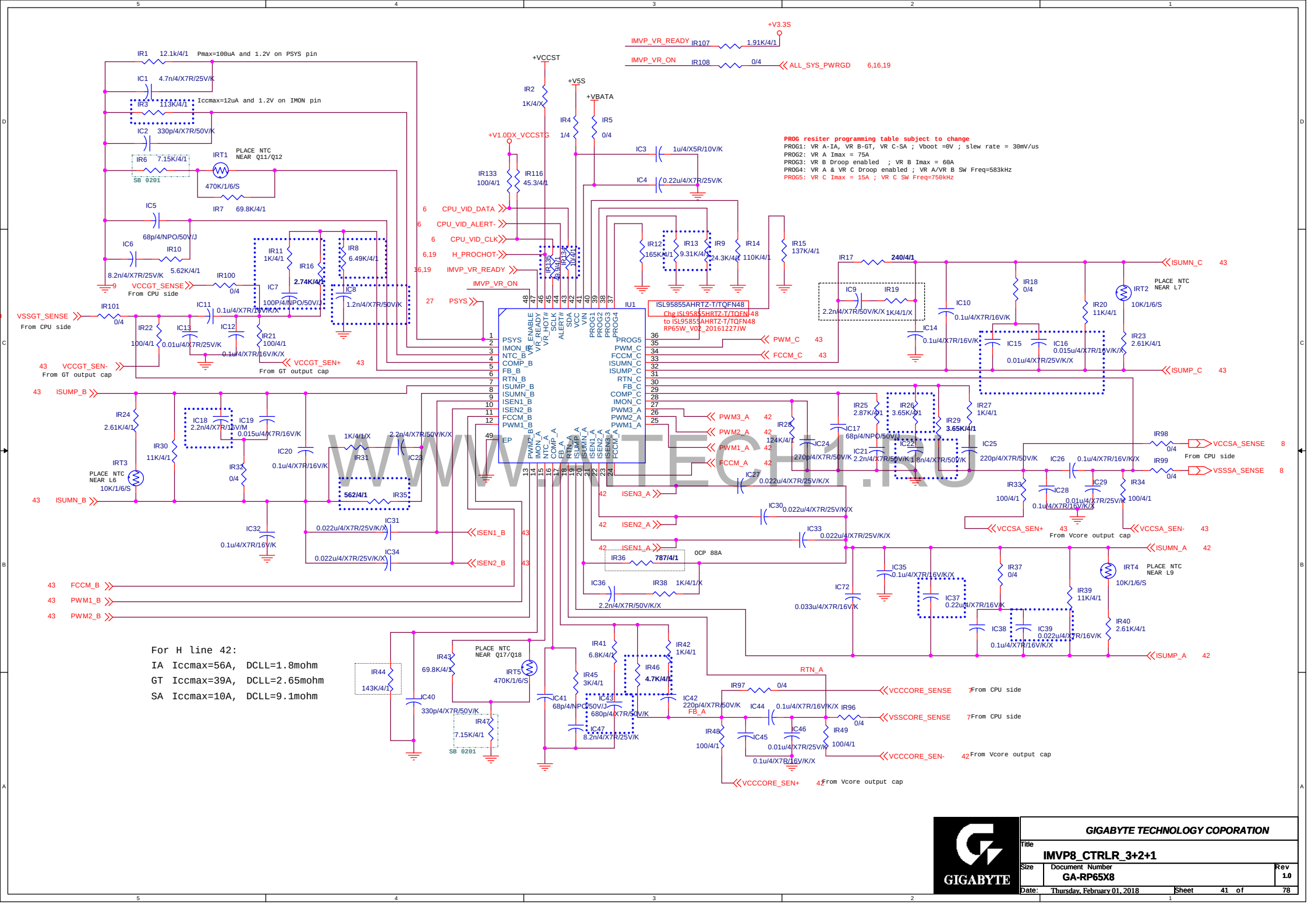

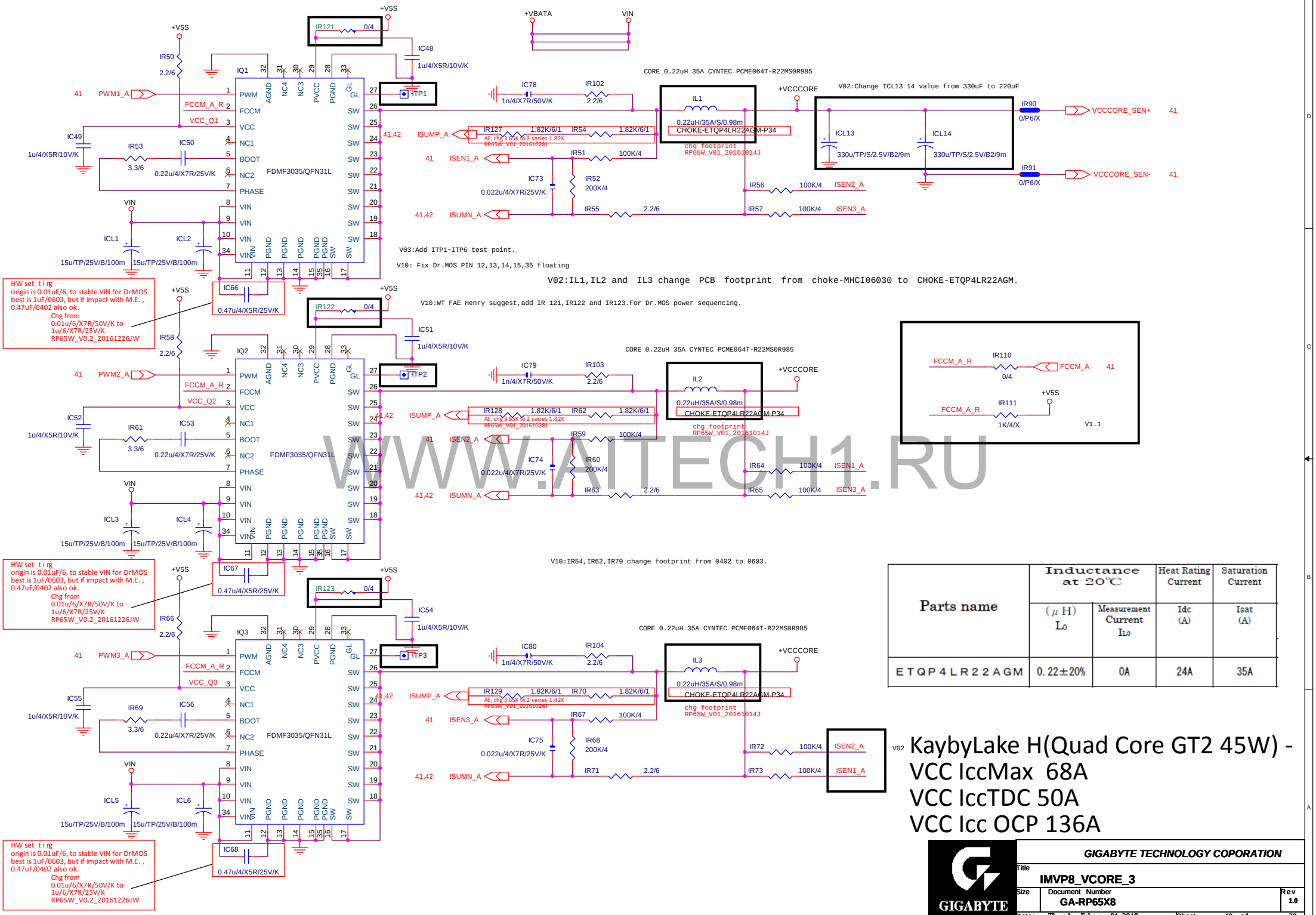

Parts name	Inductance at 20°C		Heat Rating Current	Saturation Current
	(μH) L_0	Measurement Current I_{L0}	Idc (A)	Isat (A)
ETQP4LR22AGM	0.22±20%	0A	24A	35A

V02 KaybyLake H(Quad Core GT2 45W) -
VCC IccMax 68A
VCC IccTDC 50A
VCC Icc OCP 136A

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Title: IMVP8_VCORE_3

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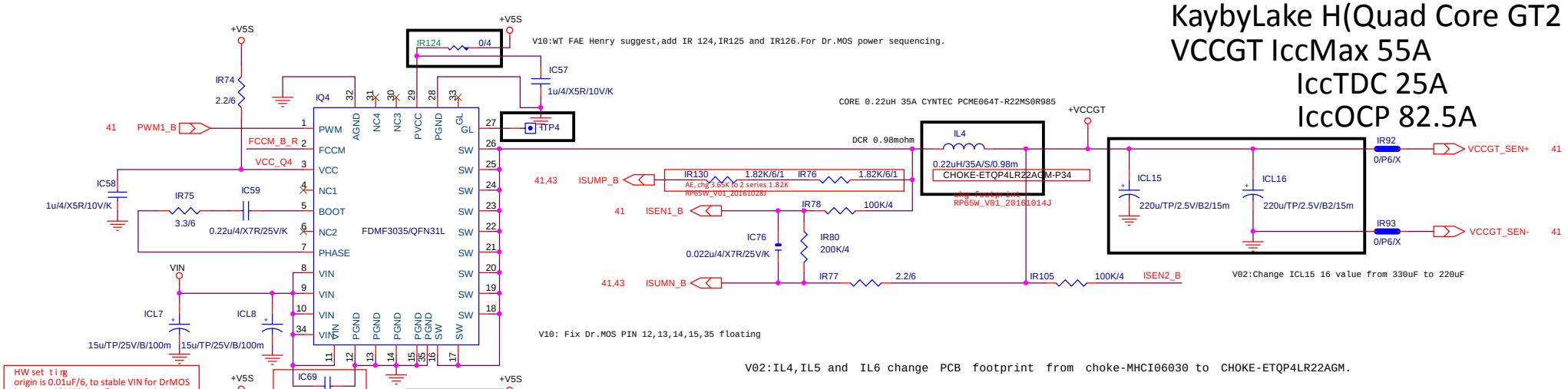
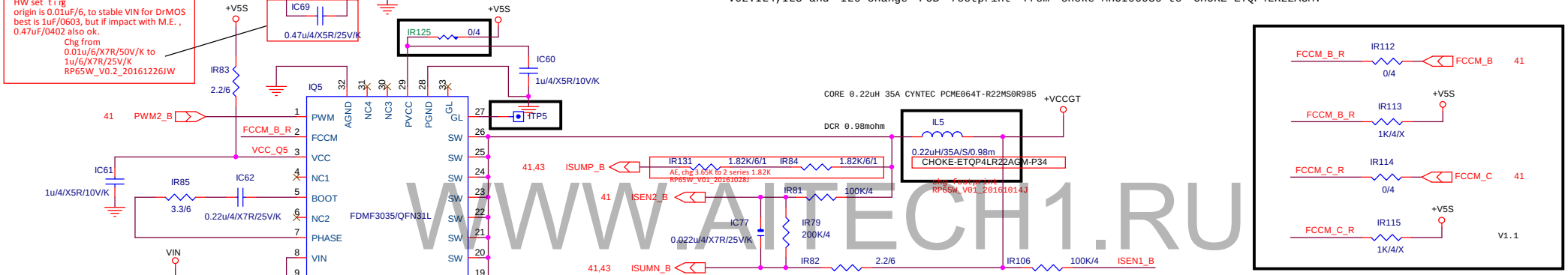
KaybyLake H(Quad Core GT2 45W) - VCCGT IccMax 55A
IccTDC 25A
IccOCP 82.5A

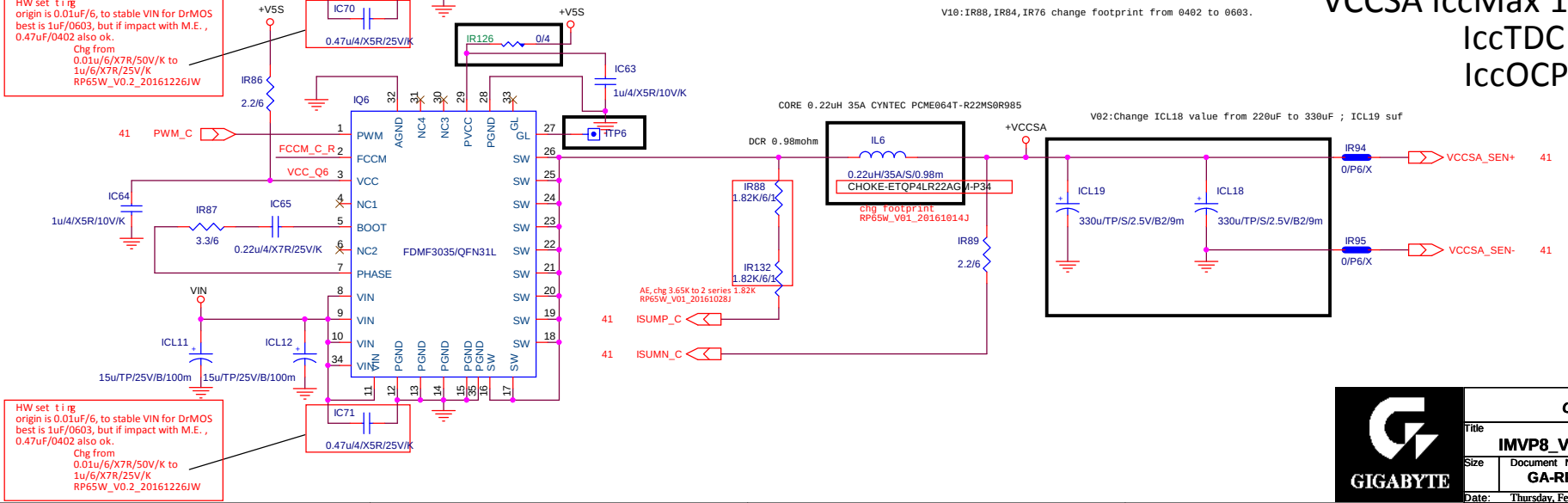


V02:IL4,IL5 and IL6 change PCB footprint from choke-MHCI06030 to CHOKE-ETQP4LR22AGM.



V10:IR88,IR84,IR76 change footprint from 0402 to 0603.

KaybyLake H(Quad Core GT2 45W) - VCCSA IccMax 11.1A
IccTDC 10A
IccOCP 16.65A



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Title: IMVP8_VGT_VSA_2+1

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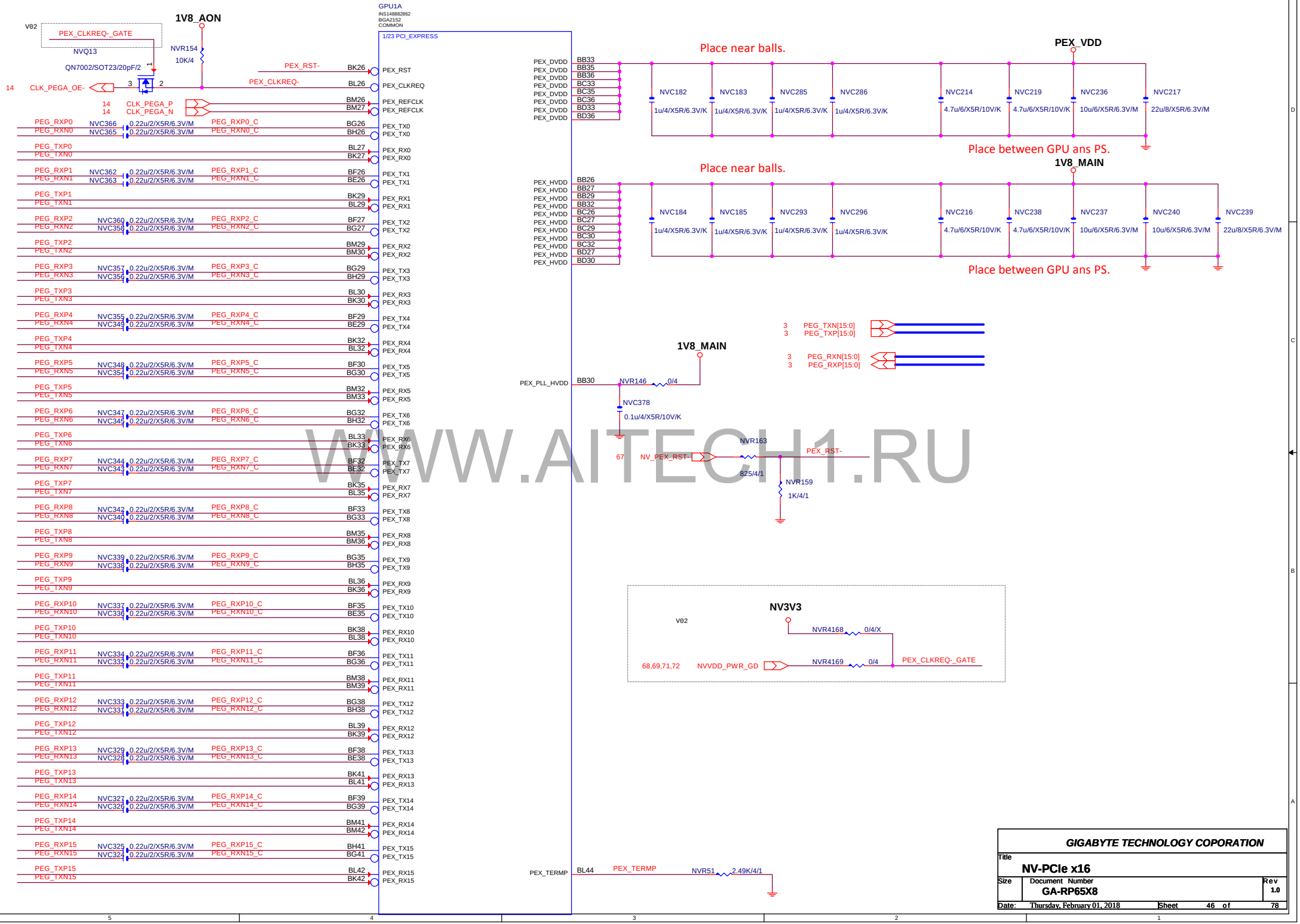
GPU1A
INS148882862
BGA2152
COMMON
1/23 PCI_EXPRESS
1V8_AON
V02
PEX_CLKREQ-_GATE
NVQ13
NVR154
10K/4
QN7002/SOT23/20pF/2
CLK_PEGA_OE-
PEX_RST-
PEX_CLKREQ-
CLK_PEGA_P
CLK_PEGA_N
PEX_RST
PEX_CLKREQ
PEX_REFCLK
PEX_VDD
Place near balls.
Place between GPU ans PS.
1V8_MAIN
PEX_HVDD
PEX_PLL_HVDD
NVR146
0/4
NVC378
0.1u/4/X5R/10V/K
PEG_TXN[15:0]
PEG_TXP[15:0]
PEG_RXN[15:0]
PEG_RXP[15:0]
NV_PEX_RST-
NVR163
825/4/1
NVR159
1K/4/1
NV3V3
NVR4168
0/4/X
NVR4169
0/4
NVVDD_PWR_GD
PEX_TERMP
NVR51
2.49K/4/1
WWW.AITECH1.RU
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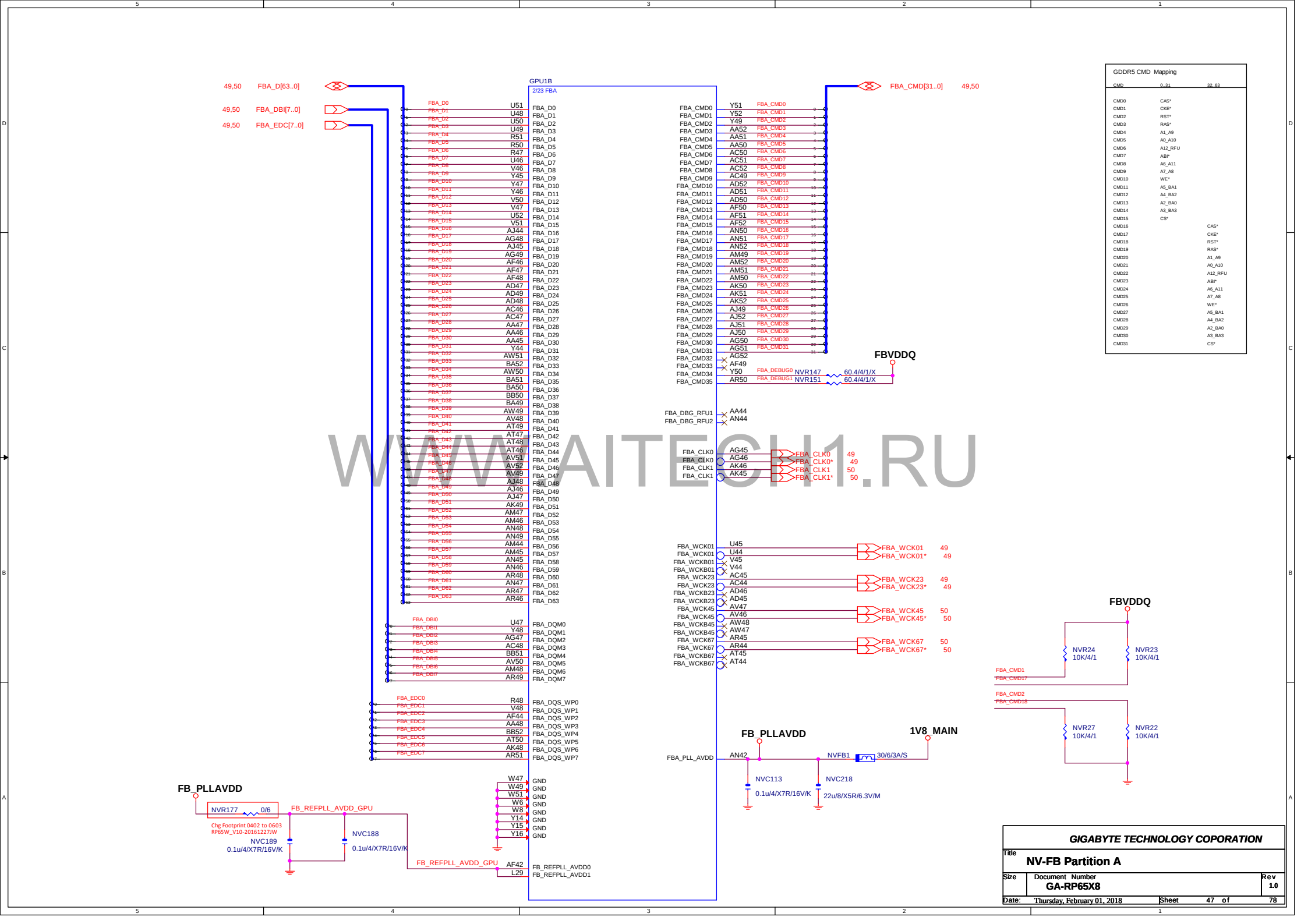

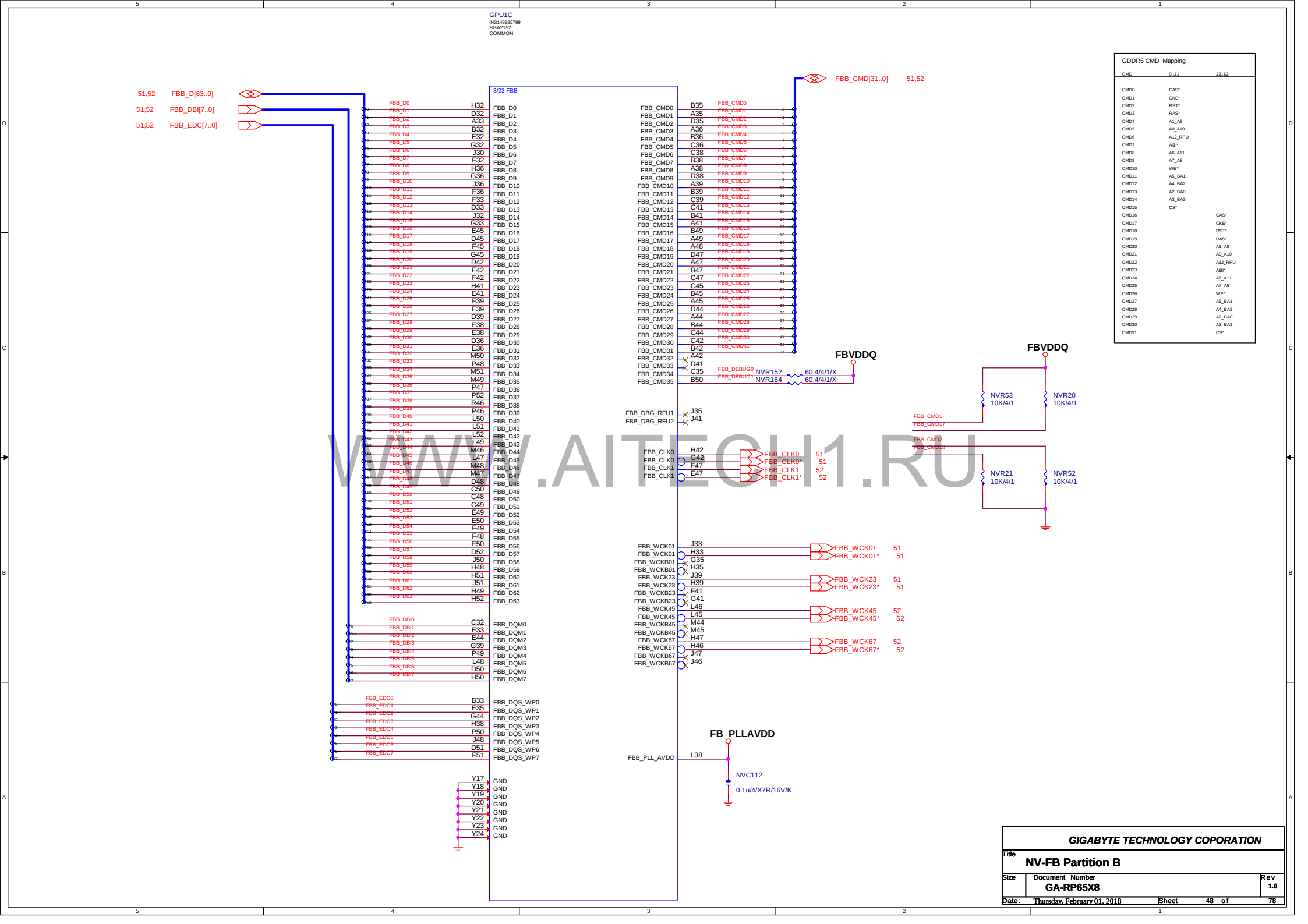

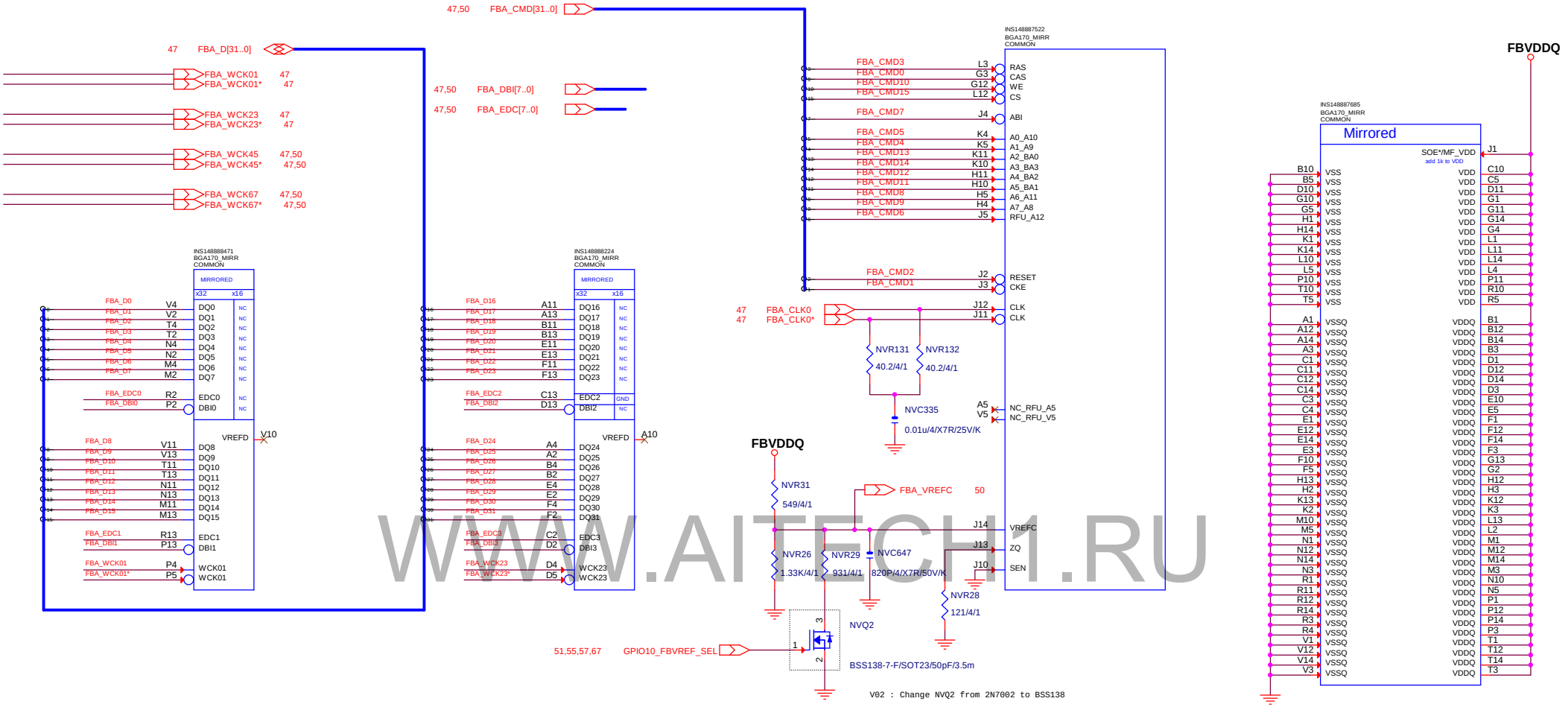

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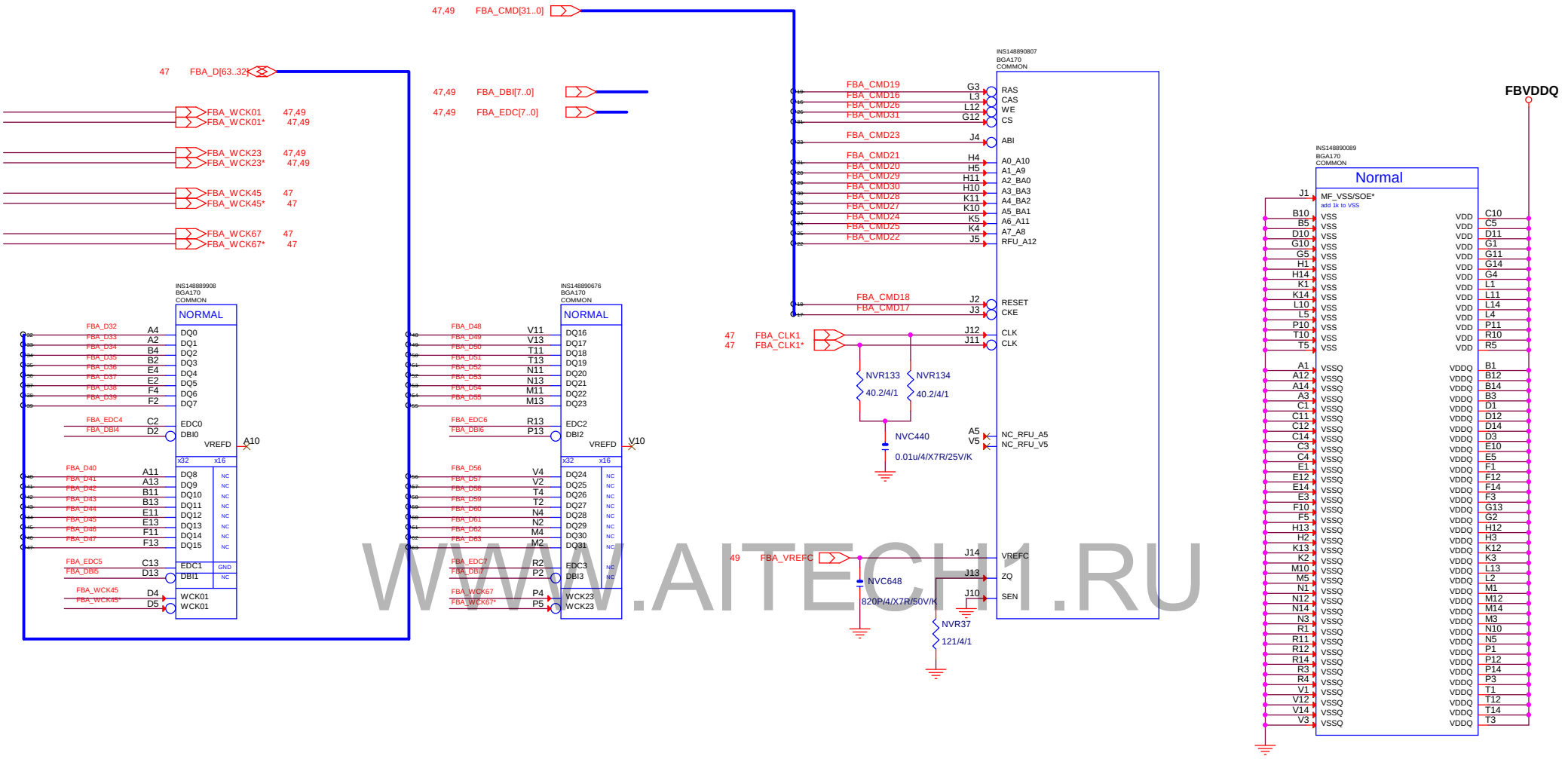

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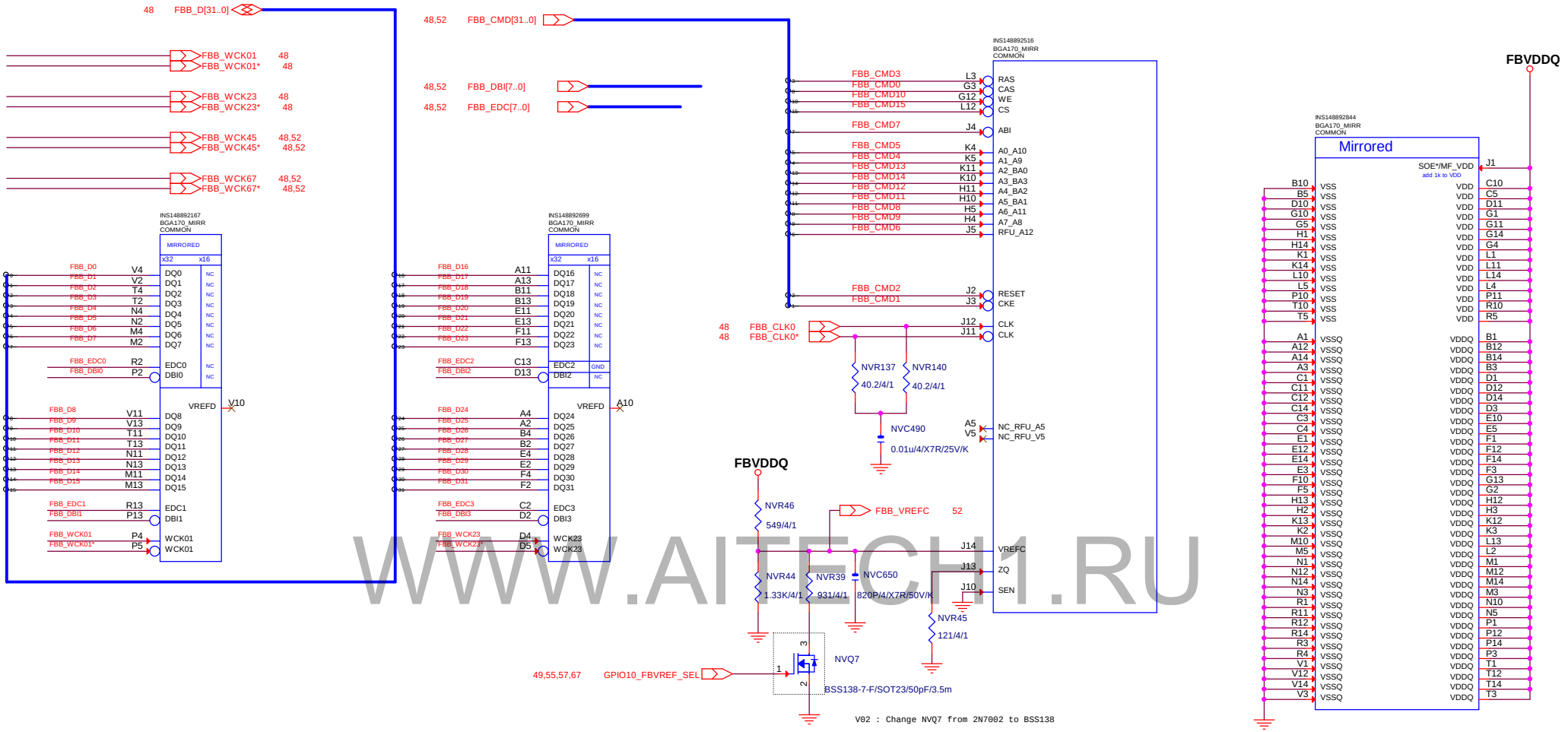

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Size	Document Number: GA-RP65X8	Rev: 1.0
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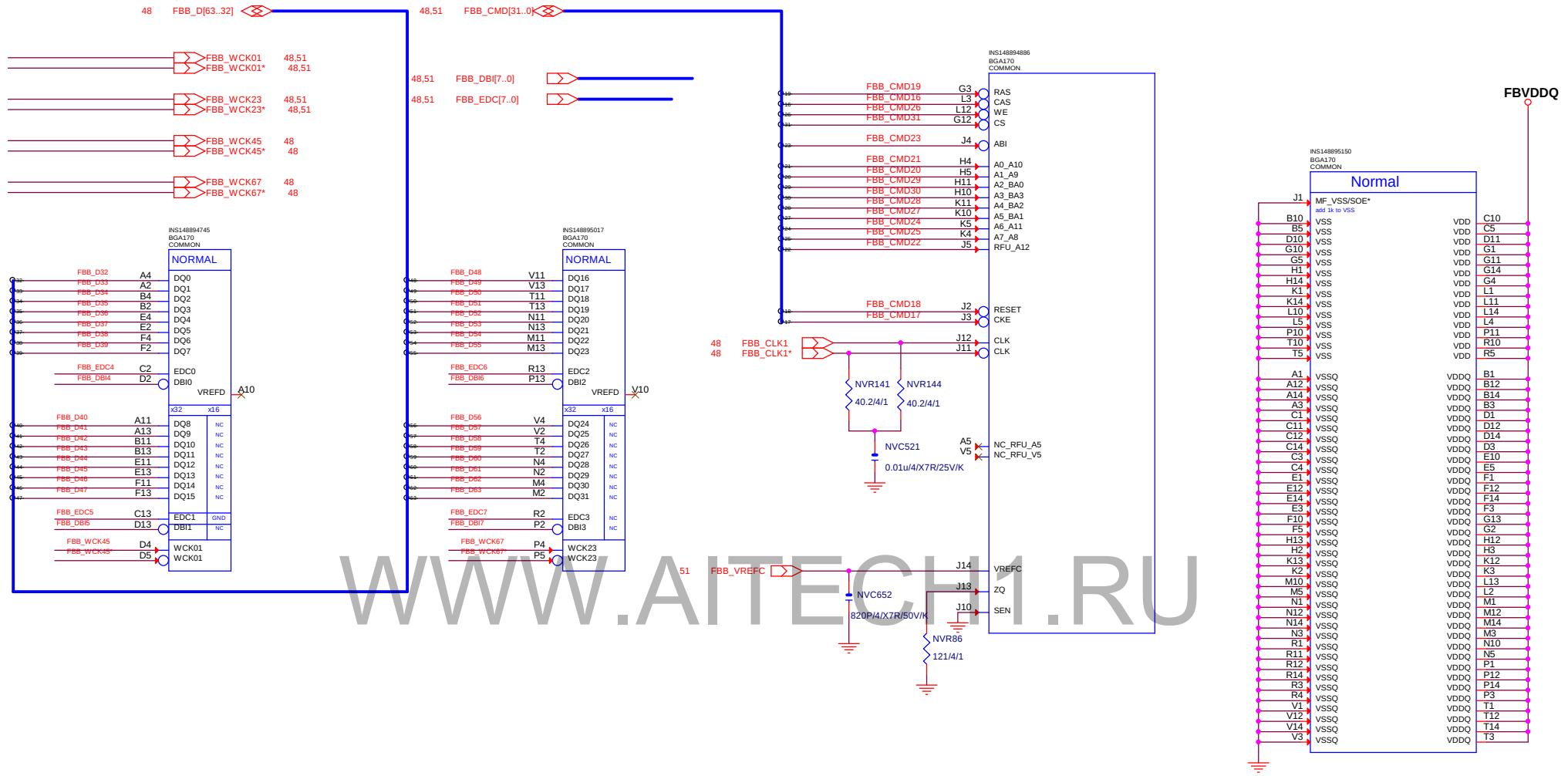

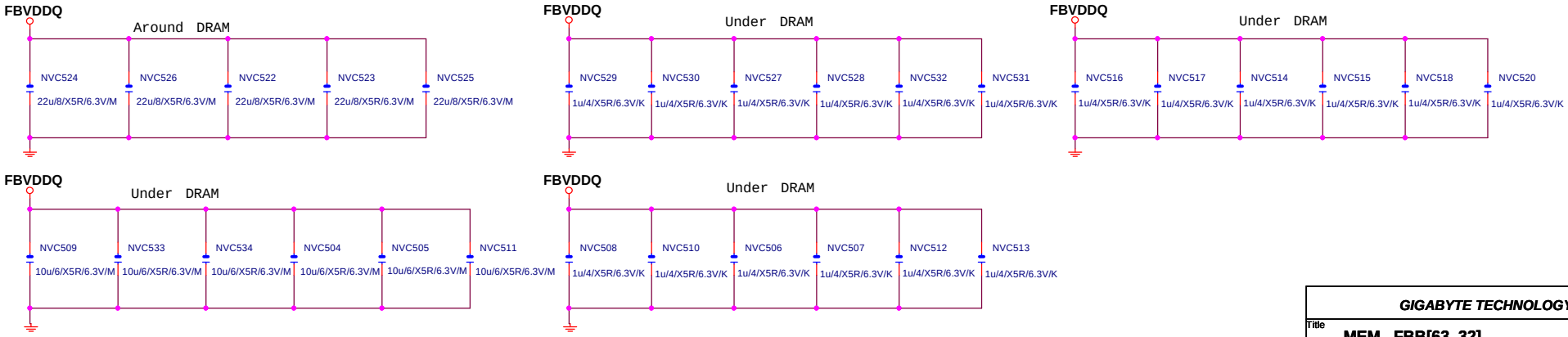

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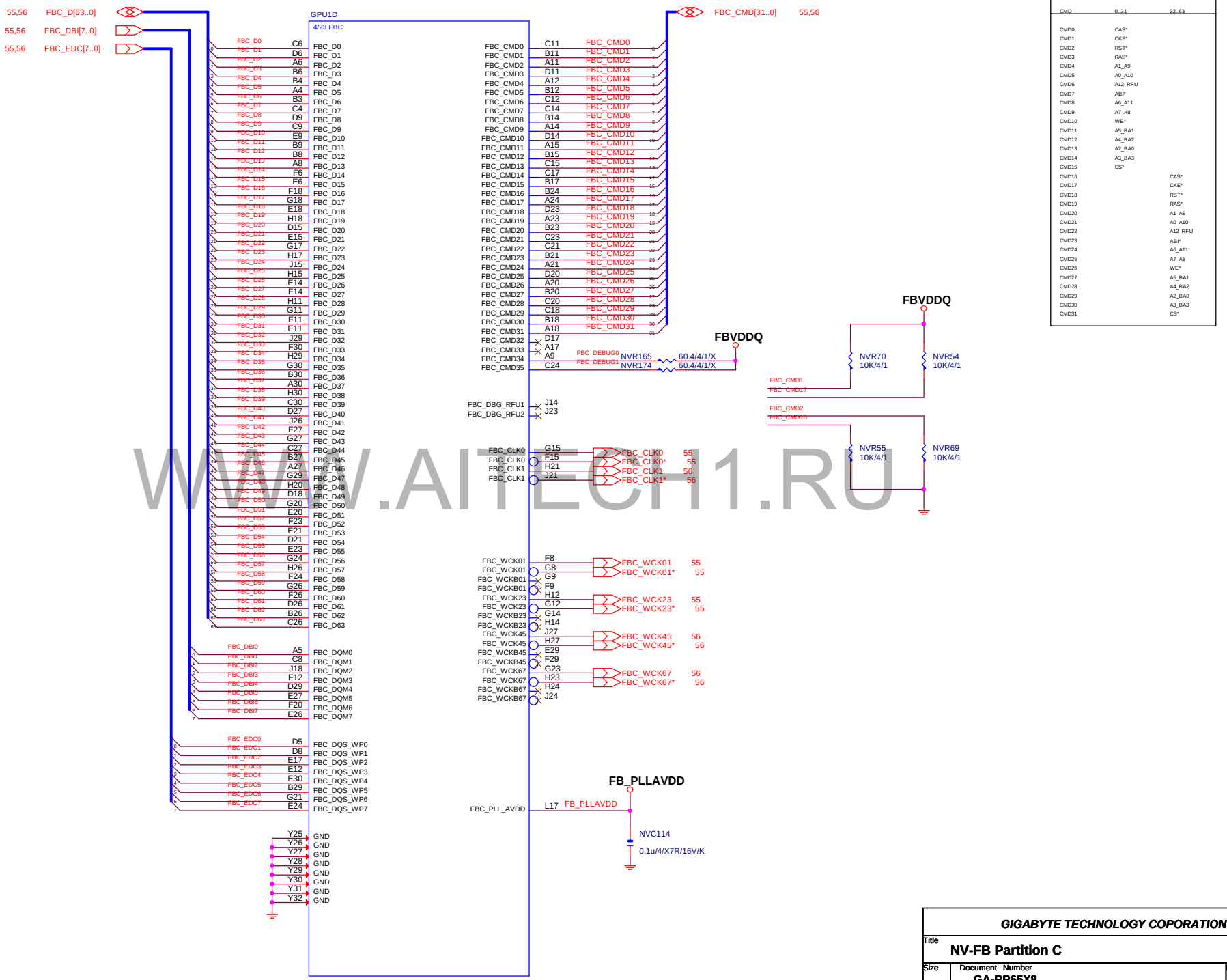

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Size	Document Number: GA-RP65X8		Rev: 1.0
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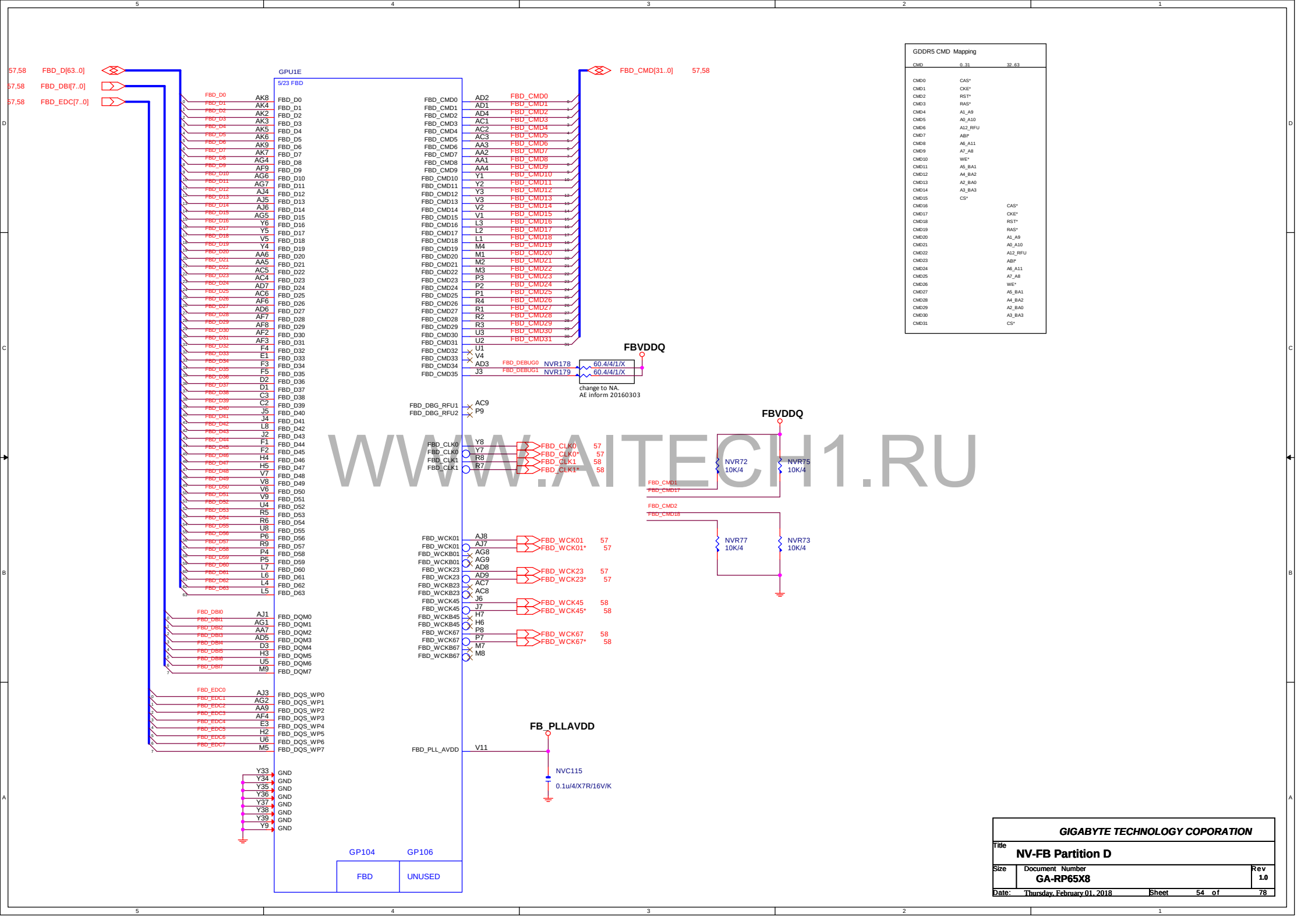

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Size	Document Number: GA-RP65X8	Rev: 1.0
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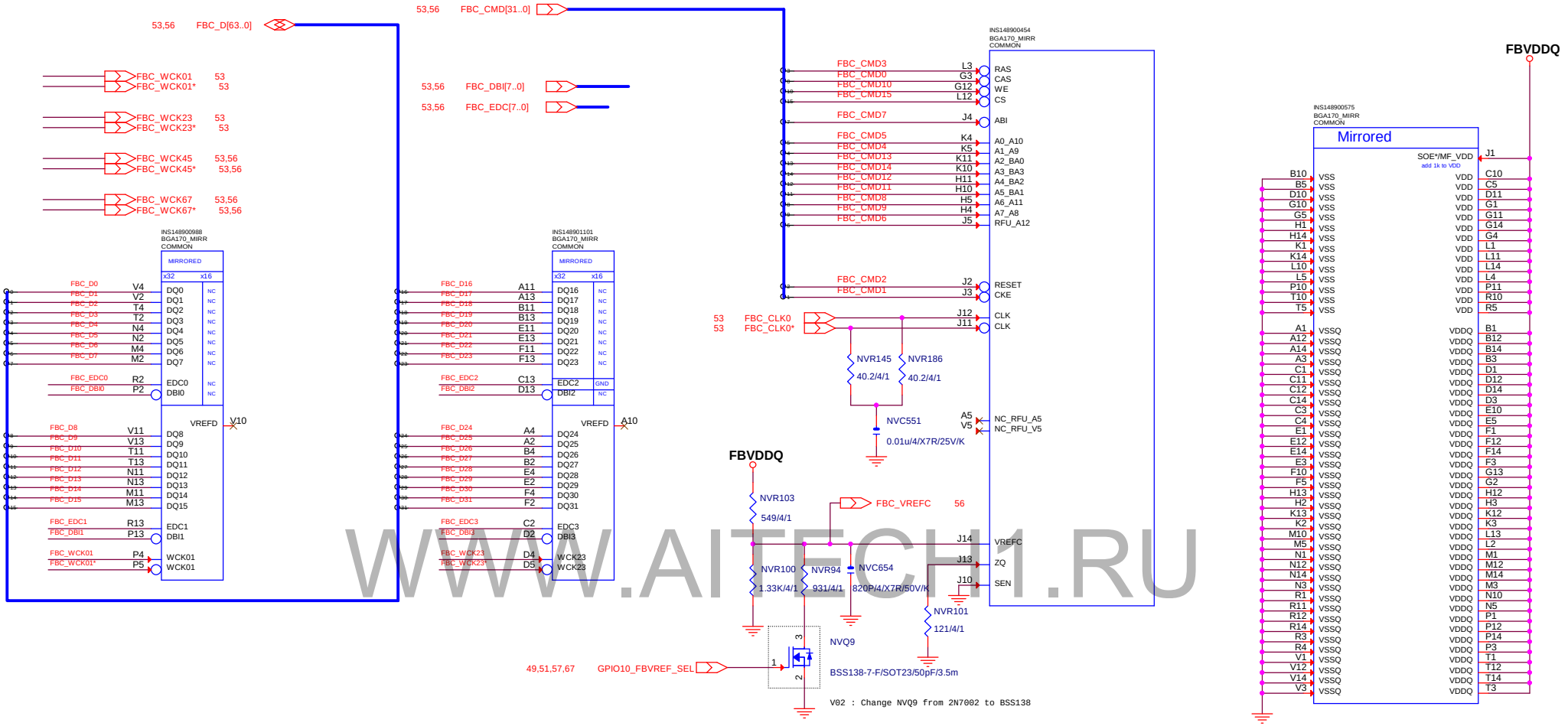

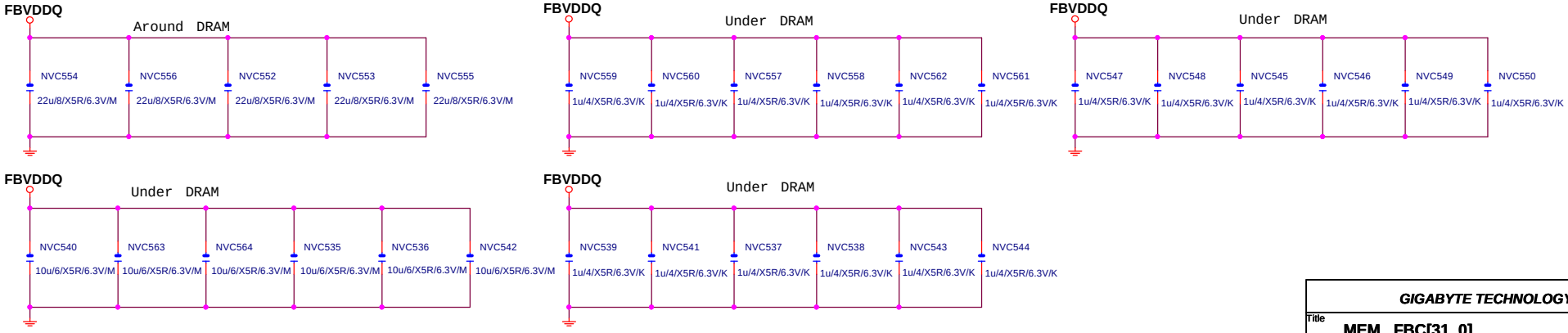

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Size	Document Number: GA-RP65X8	Rev: 1.0
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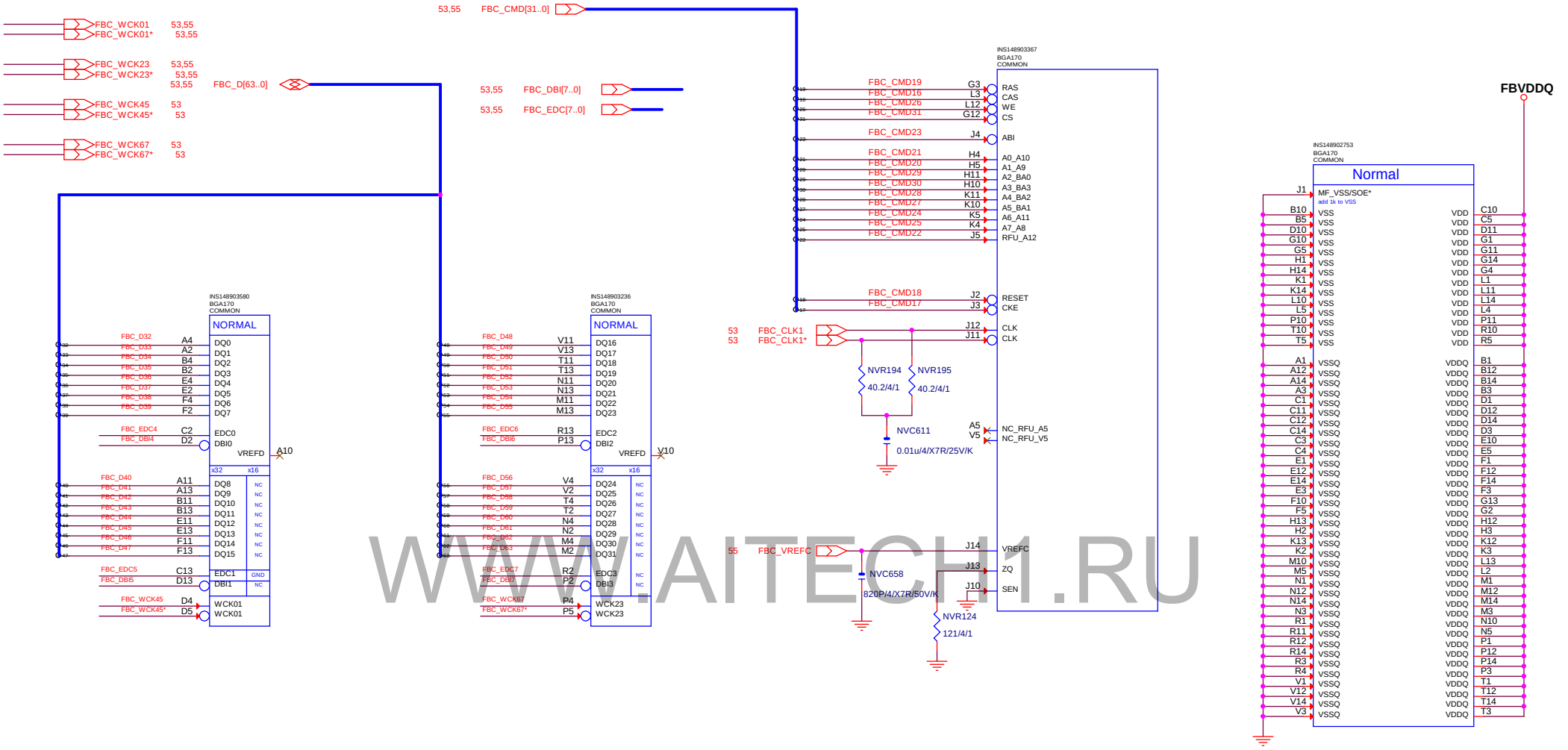

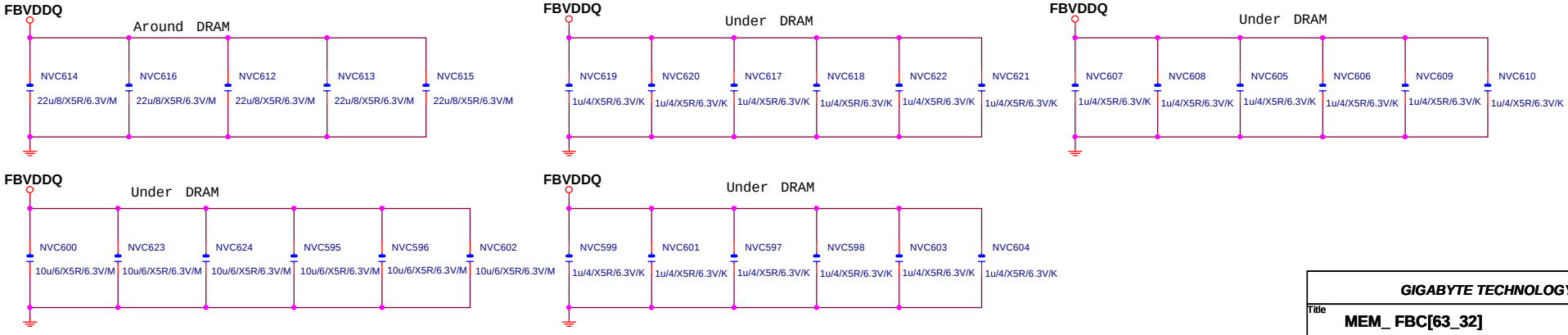

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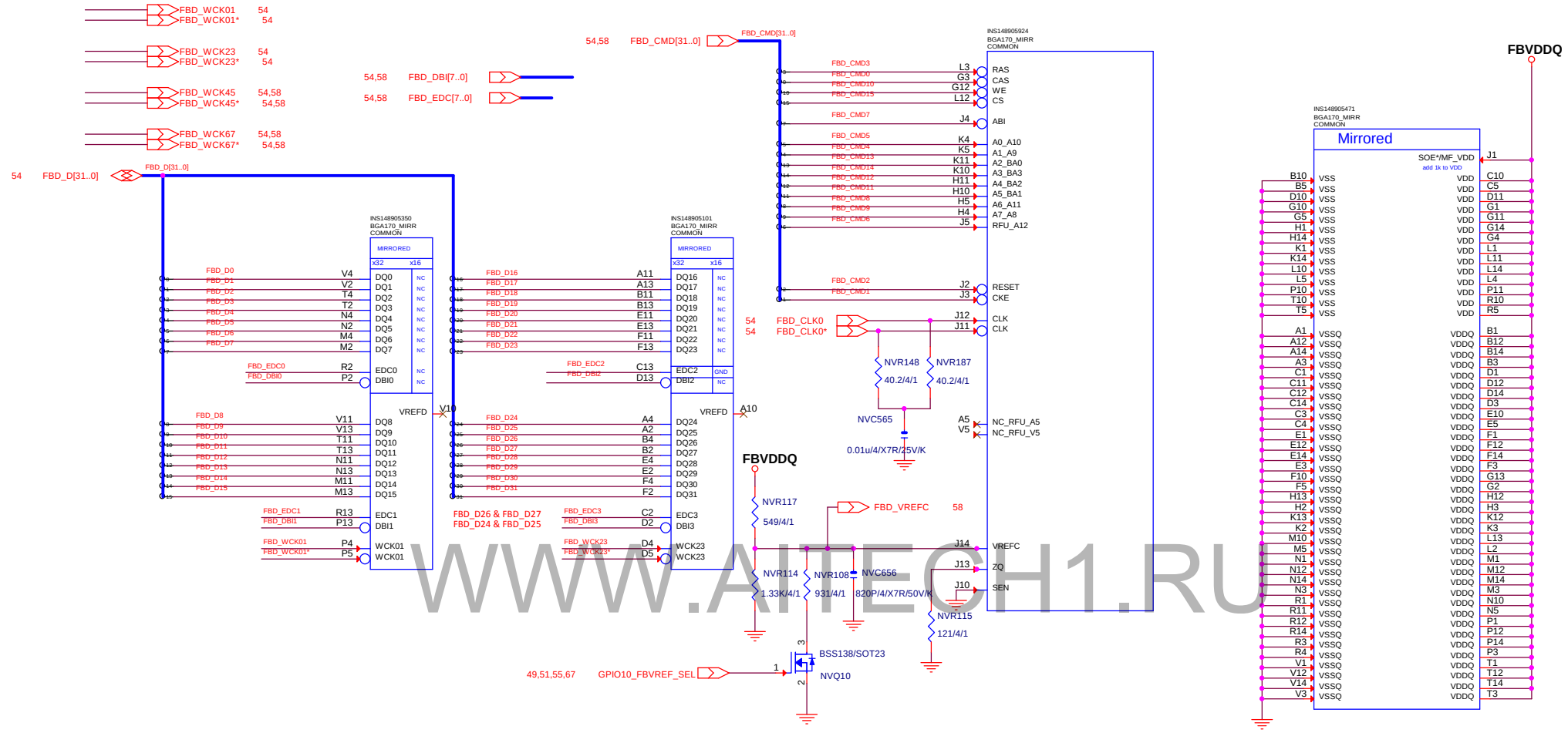

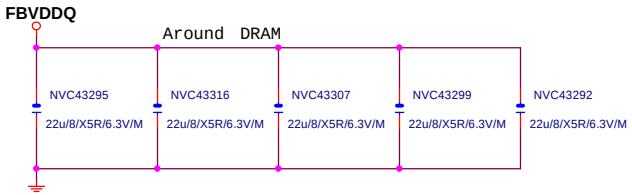

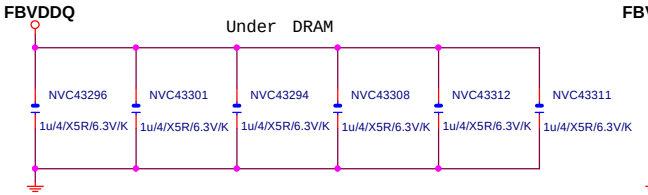

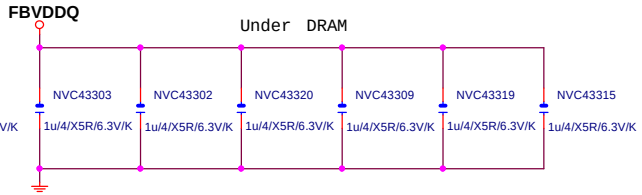

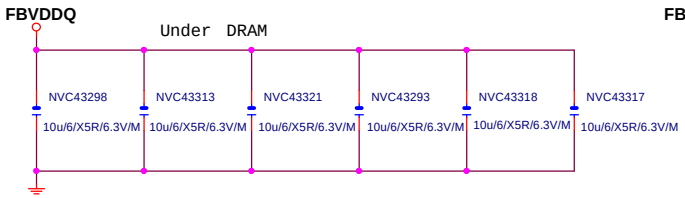

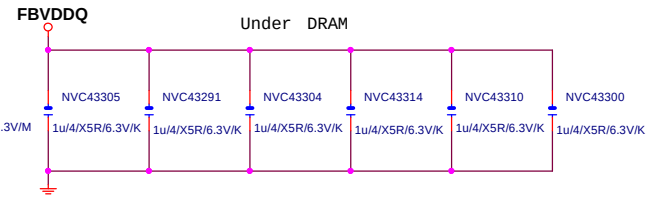

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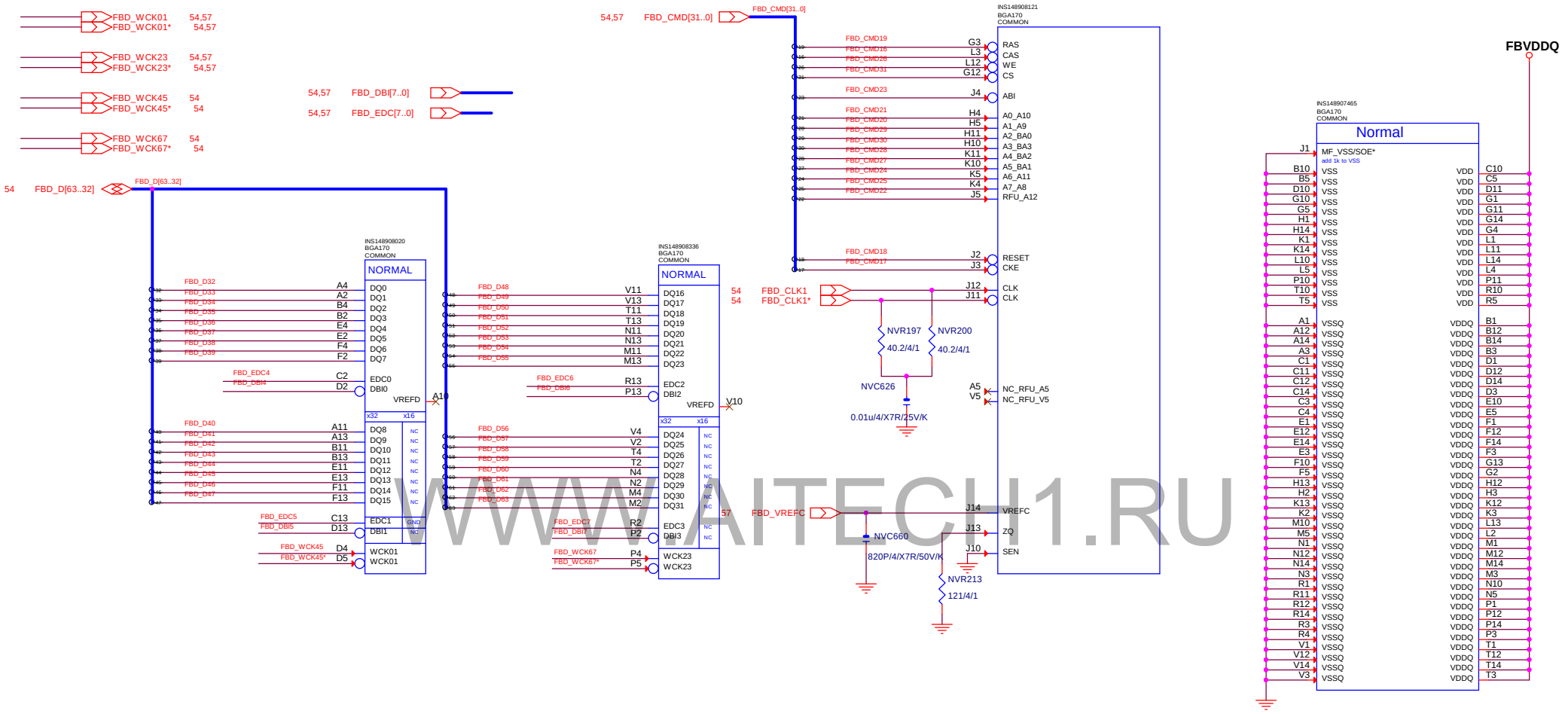

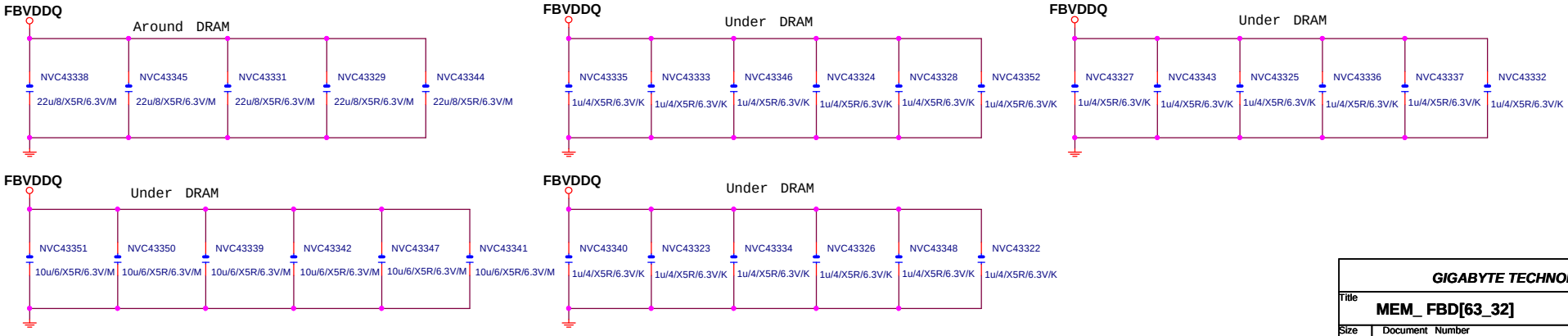

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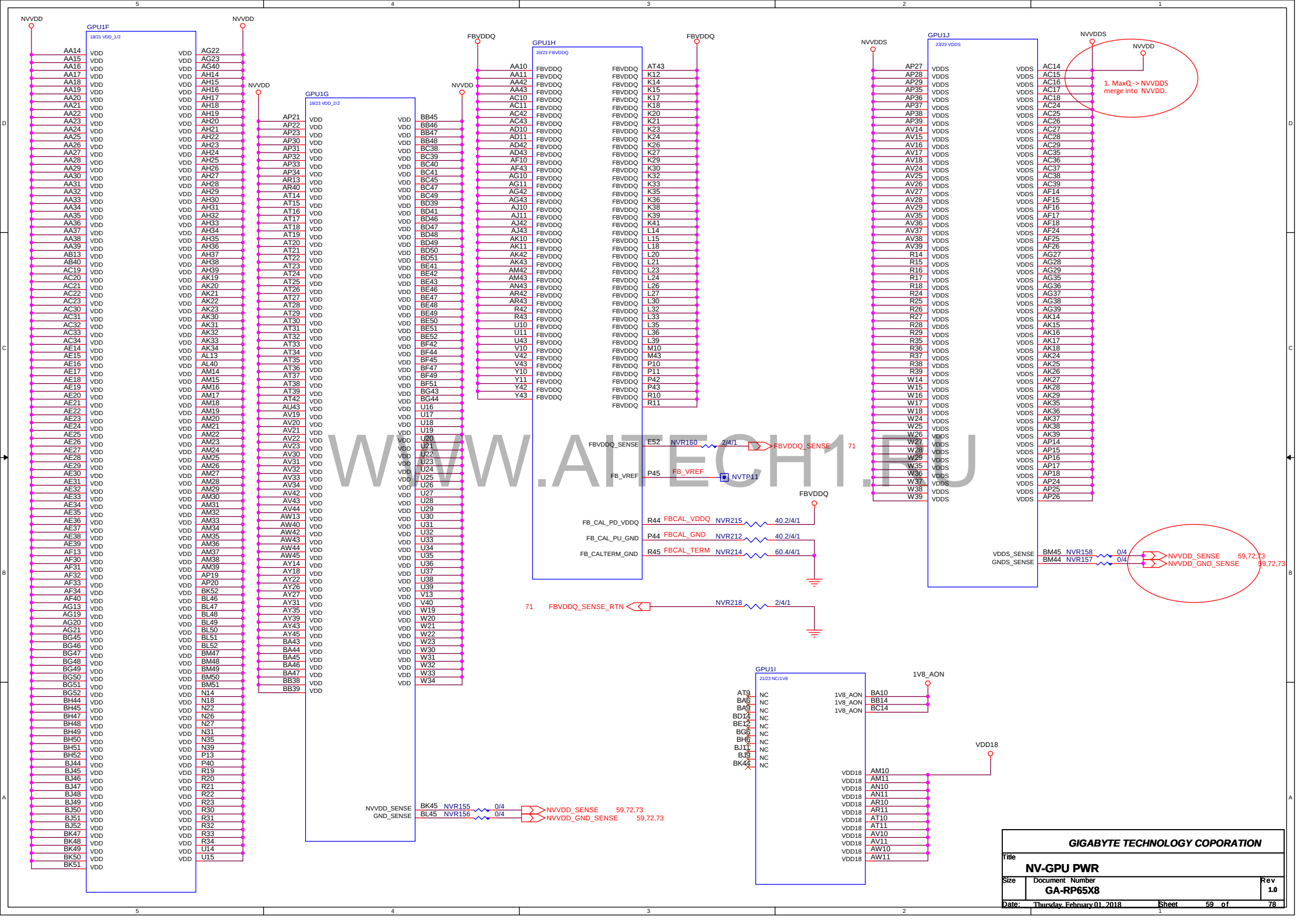

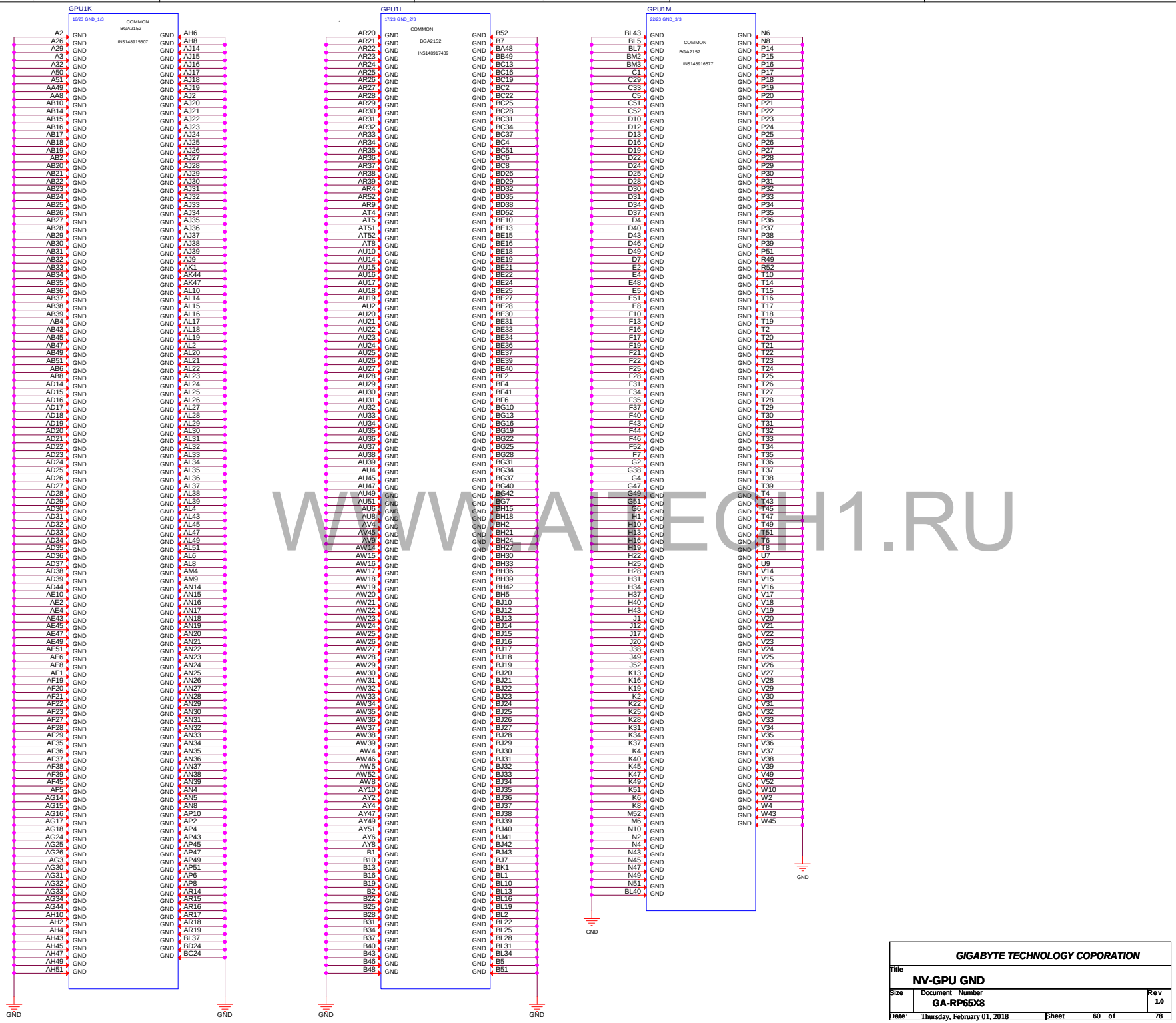

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Title: NV-GPU GND			
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GPU DECOUPLING

FBVDDQ

Partition A 2 x 10uF / 6 x 1uF — Under GPU

NVC187 NVC190 NVC198 NVC199 NVC200 NVC201 NVC288 NVC287
1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M

Partition B 2 x 10uF / 6 x 1uF — Under GPU

NVC291 NVC295 NVC202 NVC203 NVC290 NVC294 NVC292 NVC289
1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M

Partition C 2 x 10uF / 6 x 1uF — Under GPU

NVC307 NVC310 NVC299 NVC301 NVC306 NVC309 NVC308 NVC305
1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M

Partition D 2 x 10uF / 6 x 1uF — Under GPU

NVC316 NVC319 NVC311 NVC312 NVC315 NVC318 NVC317 NVC314
1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M

Place close to GPU 4 x 10uF

NVC37 NVC36 NVC76 NVC34
10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M

Place close to GPU 9 x 10uF

NVC39 NVC38 NVC77 NVC35 NVC43
22u/6/X5R/6.3V/M 22u/6/X5R/6.3V/M 22u/6/X5R/6.3V/M 22u/6/X5R/6.3V/M 22u/6/X5R/6.3V/M

Place close to GPU

NVC41 NVC40 NVC78 NVC42
22u/6/X5R/6.3V/M 22u/6/X5R/6.3V/M 22u/6/X5R/6.3V/M 22u/6/X5R/6.3V/M

Place close to GPU

NVVDDS
NVC55 47u/8/X5R/6.3V/M
NVCT3 330u/TP/S/2.5V/B2/9m
NVVDD
1. MaxQ -> NVVDDS merge into NVVDD.

NVVDD
NVCT11 330u/TP/S/2.5V/B2/9m
NVCT12 330u/TP/S/2.5V/B2/9m

NVVDDS

Under GPU

NVC86 NVC60 NVC698 NVC85
10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M

Under GPU

NVC323 NVC341 NVC320 NVC321 NVC322 NVC330 NVC346 NVC351
1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K

Under GPU

NVC369 NVC370 NVC359 NVC367 NVC364 NVC368 NVC371 NVC352
1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K 1u/4/X5R/6.3V/K

NVVDDS
16 x 1uF
4 x 10uF

NVVDD

Under GPU

NVC61 NVC58 NVC57 NVC84
10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M

Under GPU

NVC45 NVC46 NVC82 NVC47 NVC44 NVC54
47u/8/X5R/6.3V/M 47u/8/X5R/6.3V/M 22u/6/X5R/6.3V/M 22u/6/X5R/6.3V/M 22u/6/X5R/6.3V/M 22u/6/X5R/6.3V/M

Under GPU

NVC49 NVC50 NVC83 NVC51 NVC48 NVC52 NVC53
10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M 10u/6/X5R/6.3V/M

49 x 1uF
11 x 10uF
4 x 22uF
2 x 47uF
2 x 330uF

NVVDD NVCT2 330u/TP/S/2.5V/B2/9m
NVVDD NVCT1 330u/TP/S/2.5V/B2/9m

Under GPU x49 1uF X7R 0402

NVC241 NVC244 NVC243 NVC245 NVC220 NVC222 NVC215 NVC242 NVC221 NVC223
NVC251 NVC254 NVC253 NVC255 NVC247 NVC249 NVC246 NVC252 NVC248 NVC250
NVC261 NVC264 NVC263 NVC265 NVC257 NVC259 NVC256 NVC262 NVC258 NVC260
NVC233 NVC232 NVC231 NVC230 NVC229 NVC228 NVC227 NVC226 NVC225
NVC213 NVC212 NVC211 NVC210 NVC209 NVC208 NVC207 NVC206 NVC205 NVC204
1u/4/X5R/6.3V/K

VDD18

NVC66 NVC68 NVC67 NVC69
4.7u/6/X5R/10V/K 1u/4/X5R/6.3V/K 0.1u/4/X7R/16V/K 0.1u/4/X7R/16V/K

VDD18

NVC70 NVC72 NVC71 NVC73
4.7u/6/X5R/10V/K 1u/4/X5R/6.3V/K 0.1u/4/X7R/16V/K 0.1u/4/X7R/16V/K

1V8_MAIN — NVR273 0/8 — VDD18

1V8_AON

place 1 x 0.1uF cap near BA10

NVC62 NVC63 NVC65 NVC64
4.7u/6/X5R/10V/K 1u/4/X5R/6.3V/K 0.1u/4/X7R/16V/K 0.1u/4/X7R/16V/K

VDD18

NVC74 NVC79 NVC75 NVC80 NVC81
4.7u/6/X5R/10V/K 1u/4/X5R/6.3V/K 0.1u/4/X7R/16V/K 0.1u/4/X7R/16V/K 0.1u/4/X7R/16V/K

place 1 x 0.1uf cap for BB14 and BC14 to share

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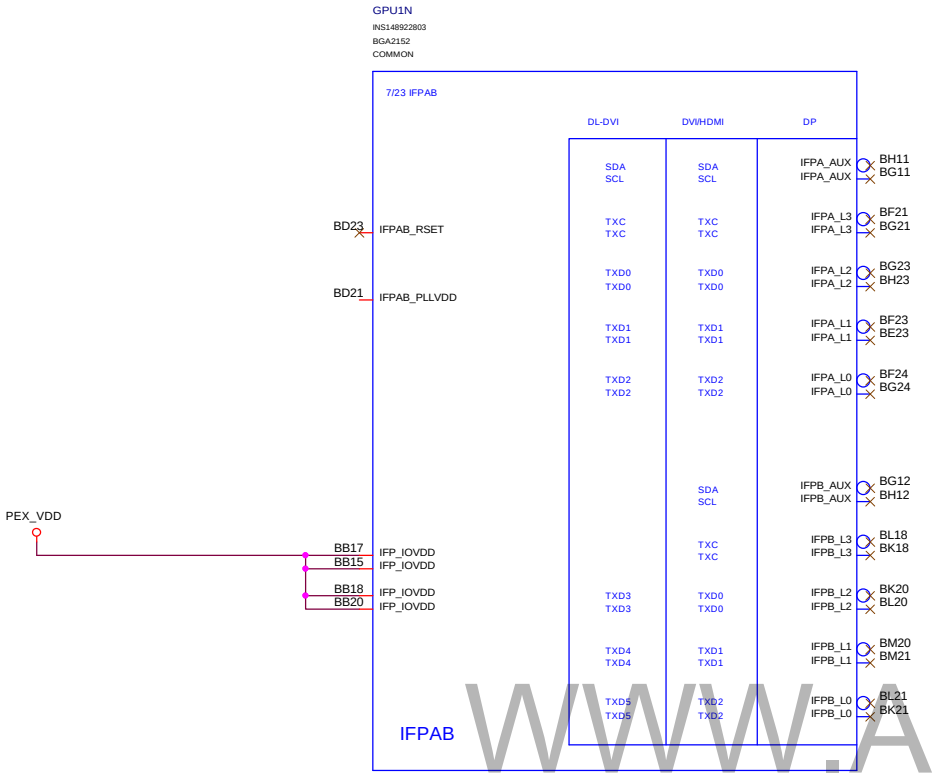

Table 10. NVVDD Voltage Regulator Requirements

Feature	Guidance
Regulator Solution Index	• N17E-G3: OVR4+ 4ph-2xDualFET/ph L=13x13x4 Lsat=70A or better • N17E-G2: OVR2+ 3ph-DualFET/ph L=10x10x4 Lsat=68A/ph or better • N17E-G1: OVR2+ 3ph-DualFET/ph L=10x10x4 Lsat=68A/ph or better
Load line	No
Low Power Mode	AutoPSI integrated in OVR4+ and OVR2+
PDN Specification (DC)	TBD
Overall Efficiency	• N17E-G3: 80% or better at EDPc = 121A • N17E-G2: 80% or better at EDPc = 80A • N17E-G1: 80% or better at EDPc = 62A

Table 11. NVVDDS Voltage Regulator Requirements

Feature	Guidance
Regulator Solution Index	• N17E-G3: OVR2+ 2ph-DualFET/ph L=10x10x4 Lsat=68A/ph or better • N17E-G2: OVR2+ 1ph-DualFET/ph L=10x10x4 Lsat=68A/ph or better • N17E-G1: OVR2+ 1ph-DualFET/ph L=10x10x4 Lsat=68A/ph or better
Load line	No
Low Power Mode	AutoPSI integrated in OVR4+ and OVR2+
PDN Specification (DC)	TBD
Overall Efficiency	• N17E-G3: 80% or better at EDPc = 37A • N17E-G2: 80% or better at EDPc = 26A • N17E-G1: 80% or better at EDPc = 21A

Table 12. FBVDD Voltage Regulator Requirements

Feature	Guidance
Regulator Solution Index	• N17E-G3: 1ph-DualFET/ph or better • N17E-G2: 1ph-DualFET/ph or better • N17E-G1: 1ph-DualFET/ph or better
PDN for FBVDD Power plane	TBD
Overall Efficiency	• N17E-G3: 80% or better at EDPc = 30A • N17E-G2: 80% or better at EDPc = 29A • N17E-G1: 80% or better at EDPc = 26A

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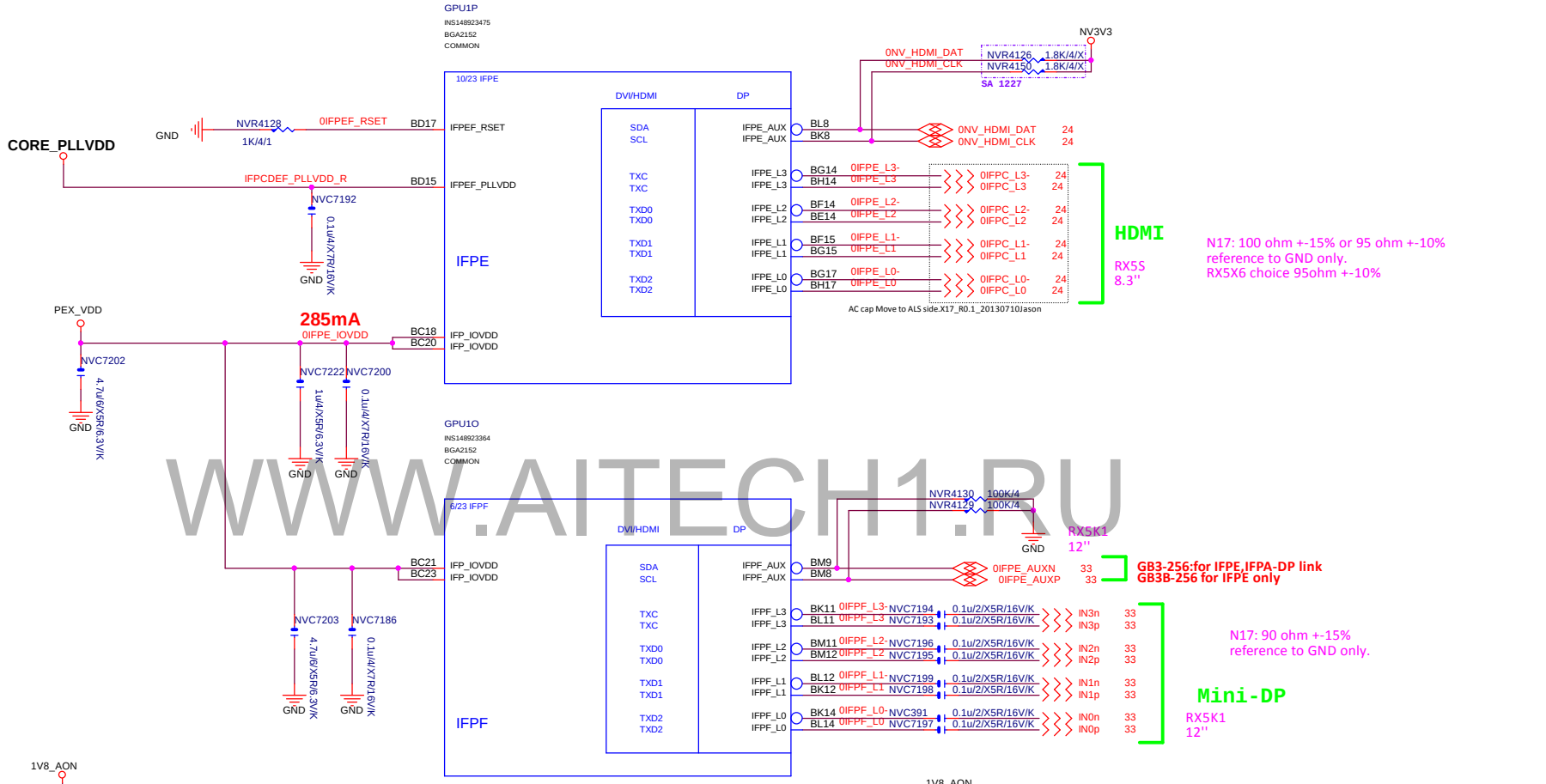
GB4-256 Split Mode EF	
Link AB	Not Connected
Link C	DisplayPort, HDMI
Link D	DisplayPort/eDP
Link E	DisplayPort, HDMI, DVI (Single Link or Dual Link)
Link F	DisplayPort/eDP, DVI (Single Link or Dual Link)
1. Only four independent display heads supported.	



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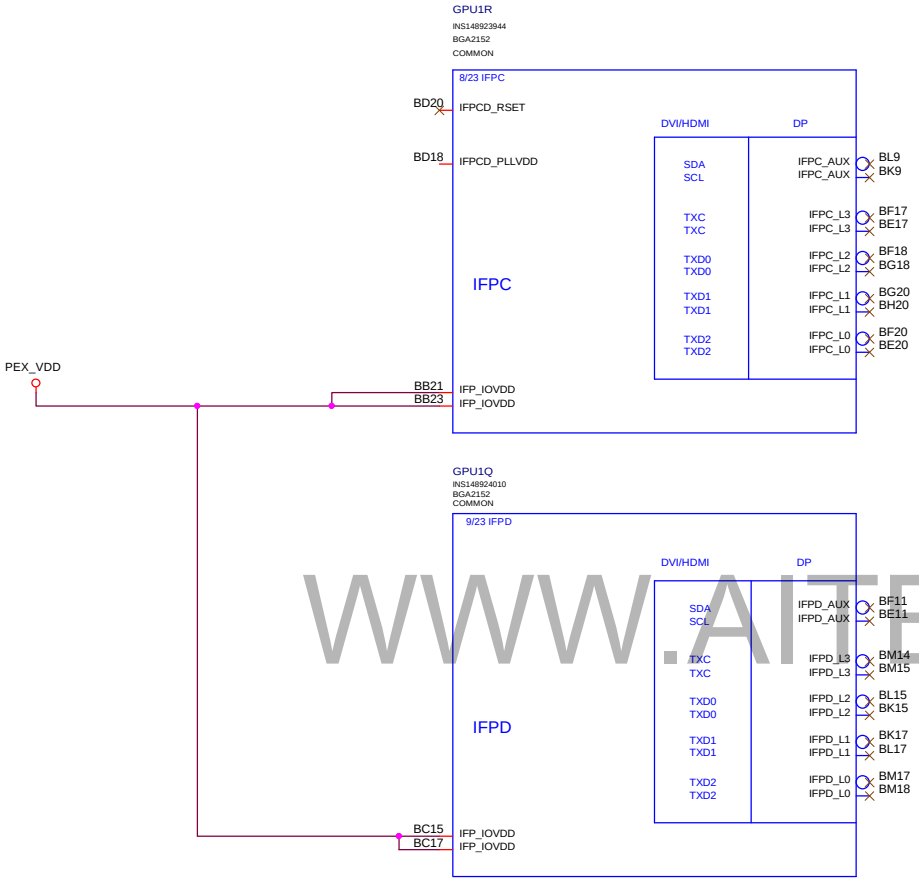

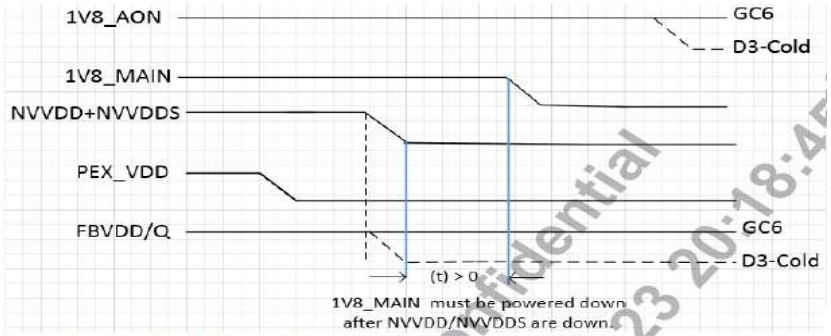

Figure 2. Example of Power-Down Sequencing Order

- NVDD, NVVDS, and PEX_VDD must power down before 1V8_MAIN, all other power rails can power down together with 1V8_MAIN.
- The propagation delay between 1V8_MAIN_EN and the NVVDD_EN pin needs to be less than 300 µs during both power up and power down.
- For GDDR5X, VPP must be equal to or higher than FBVDD/Q at all times; use gate logic and discharge circuit as needed.
- All 3.3V devices that connect to the GPU must be ramp down before 1V8_AON; GPU can NOT have any 3.3V leakage path after 1.8V_AON and 1.8V_MAIN power down.
- Power down 3V3 must be less than 10 percent before 1V8_AON can start ramp down

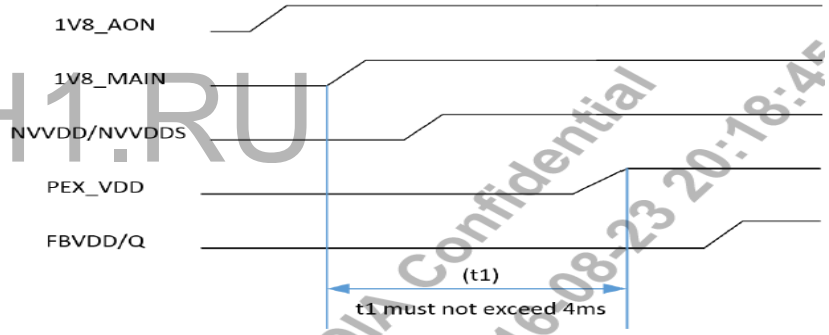

Figure 1. Example of Power-Up Sequencing Order

- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2 ms.
- t1 (from 1V8_MAIN_EN to PEX_VDD_Pgood) must *not* exceed 4 ms.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- Power up NVVDD+NVVDDS must be 90 percent before PEX_VDD can start ramp up.
- Power up 1V8_AON must be 90 percent before 3V3 ramp up
- All 3.3V devices that connect to the GPU must be powered after 1V8_AON; GPU can NOT have any 3.3V leakage path before 1V8_AON present.
- No signal should be applied to the GPU before the power rails are fully ramped
- Refer to the JEDEC Memory Specification for memory related power sequencing.
- The propagation delay between 1V8_MAIN_EN and the NVVDD_EN pin needs to be less than 300 µs during both power up and power down.
- FBVDD/Q and 1V8_AON don't need power cycle for GC6 2.1

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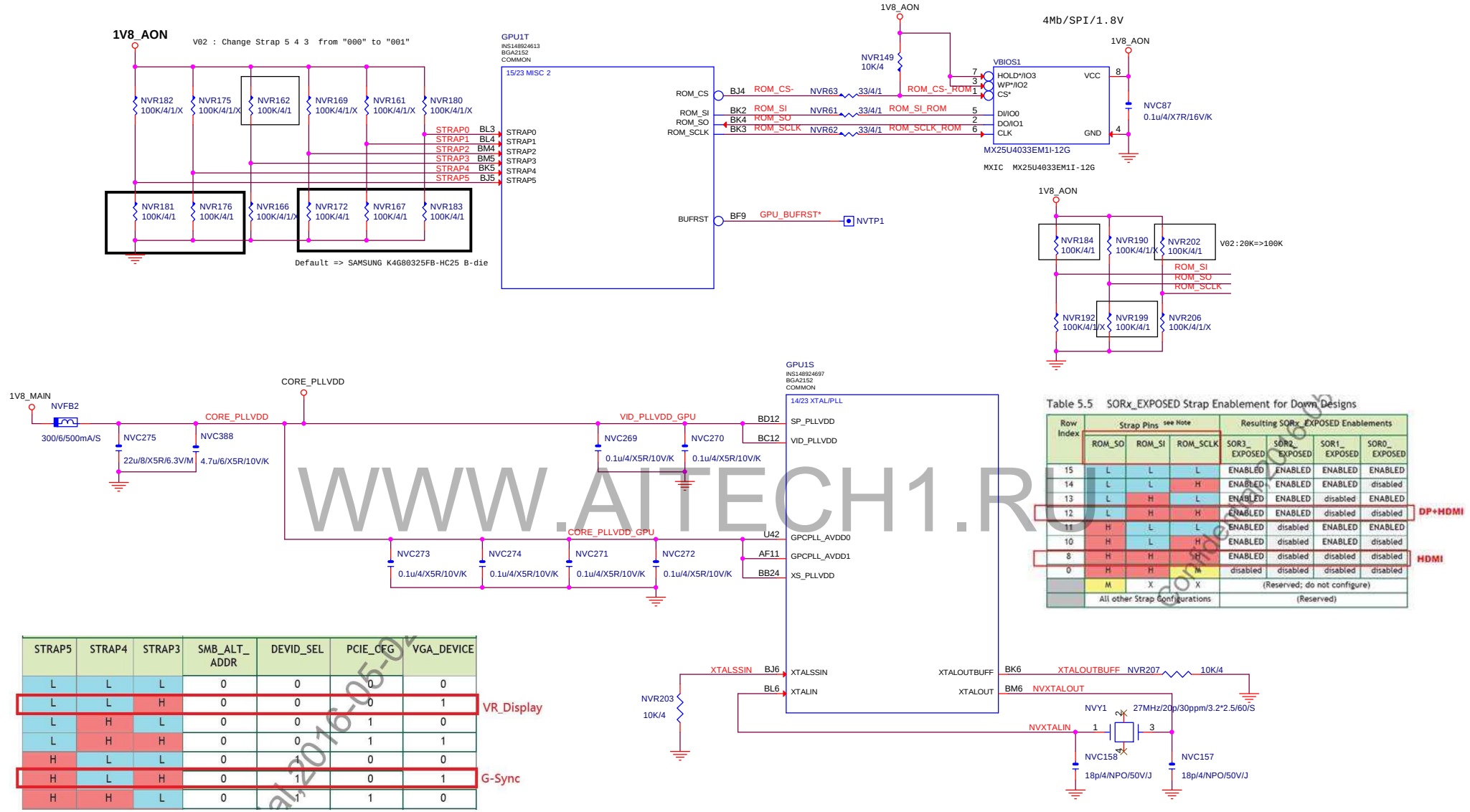

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements				
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED	
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled	
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED	
12	L	H	H	ENABLED	ENABLED	disabled	disabled	DP+HDMI
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED	
10	H	L	H	ENABLED	disabled	ENABLED	disabled	
8	H	H	L	ENABLED	disabled	disabled	disabled	HDMI
0	H	H	M	disabled	disabled	disabled	disabled	
	M	X	X	(Reserved; do not configure)				
	All other Strap Configurations			(Reserved)				

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
L	L	L	0	0	0	0	
L	L	H	0	0	0	1	VR_Display
L	H	L	0	0	1	0	
L	H	H	0	0	1	1	
H	L	L	0	1	0	0	
H	L	H	0	1	0	1	G-Sync
H	H	L	0	1	1	0	

Memory Type	FBVDD/ FBVDDQ	Memory Density	Allowed Memory Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V and 1.55V/ 1.55V See Note 2	8 Gb	256Mx32	Samsung	K4G80325FB-HC25	B-die	0x0	4000	N/A	Production candidate
				Micron	MT51J256M32HF-80:A	A-die	0x1	4000	N/A	Production candidate
				Hynix	H5GQ8H24MJR-R4C	M-die	0x2	4000	N/A	Post-production candidate

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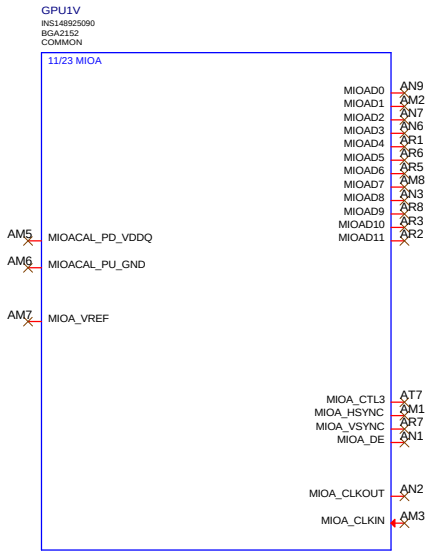

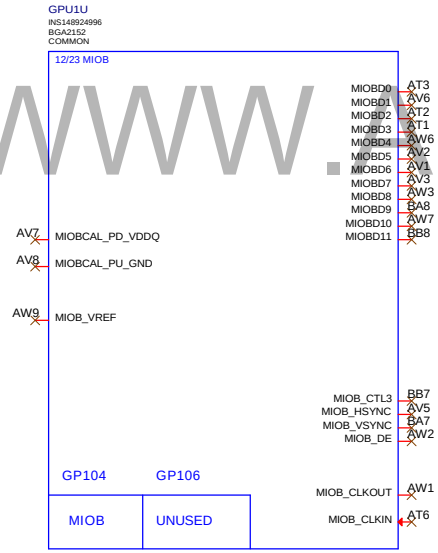

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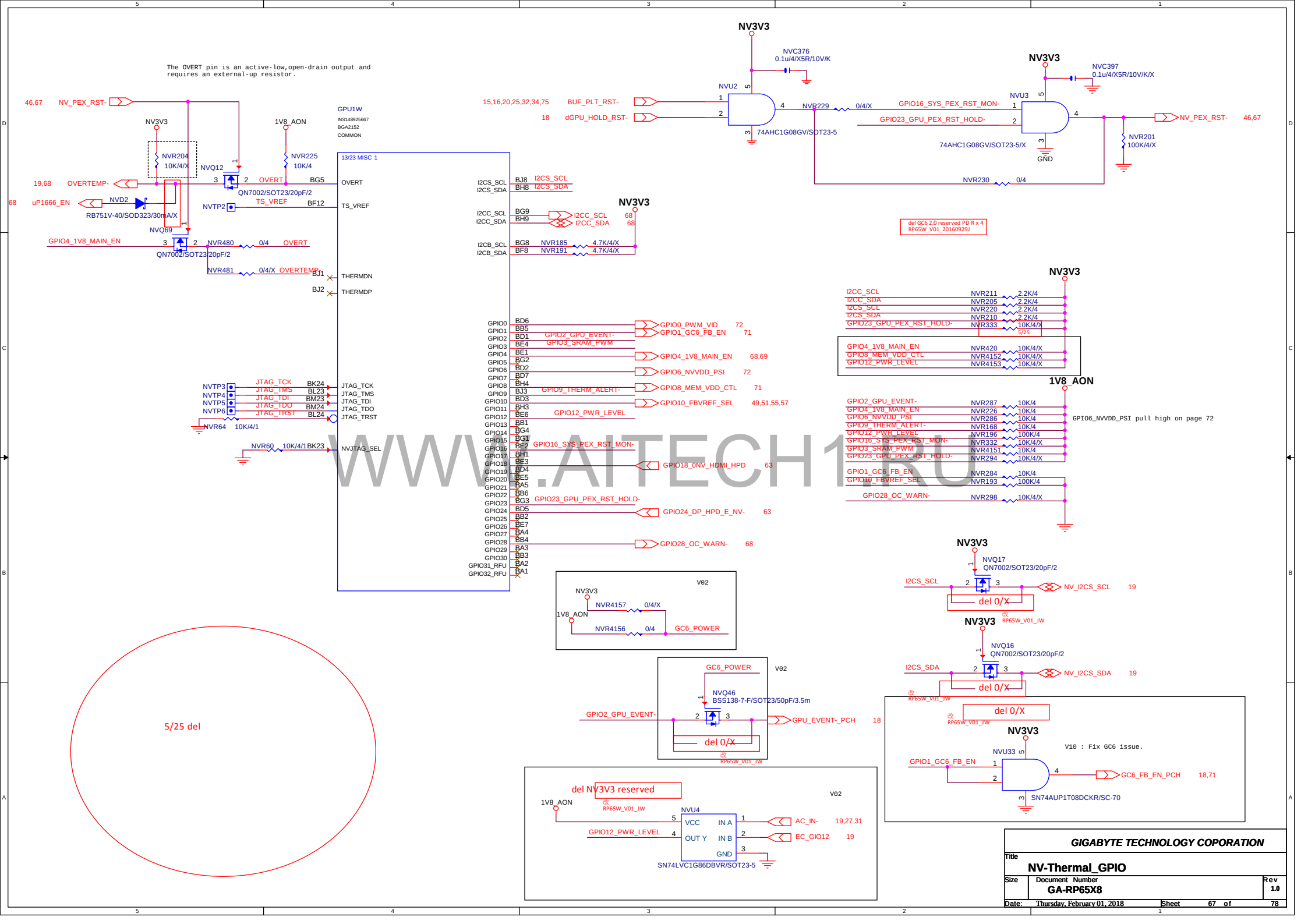
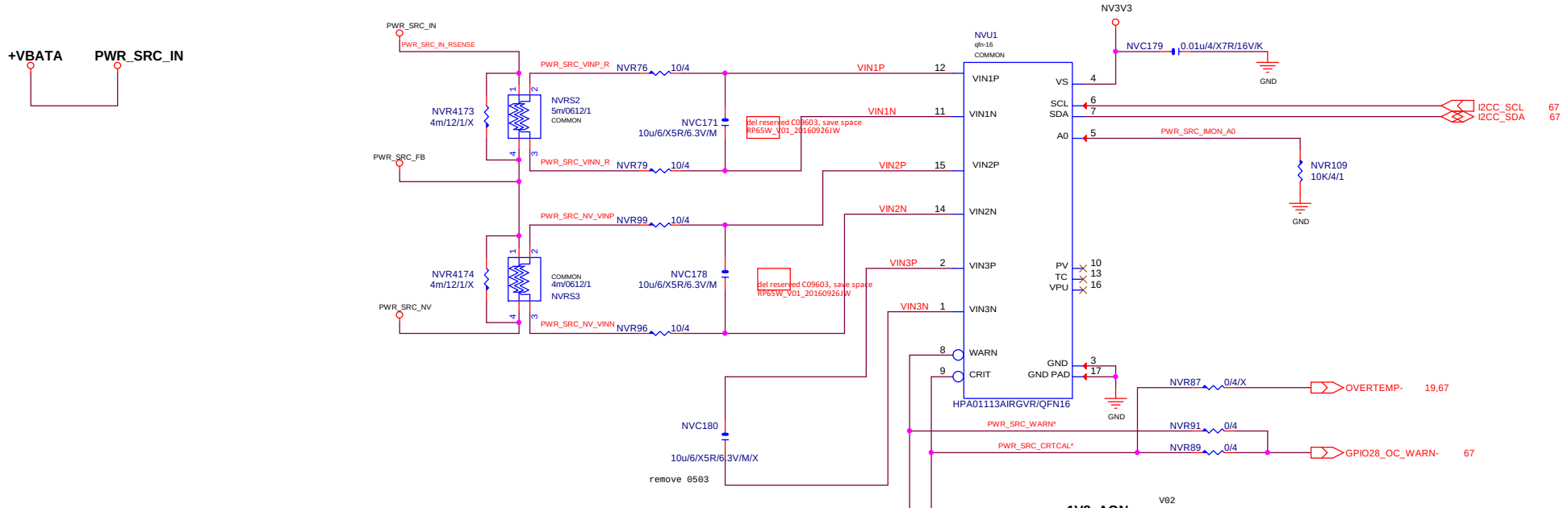
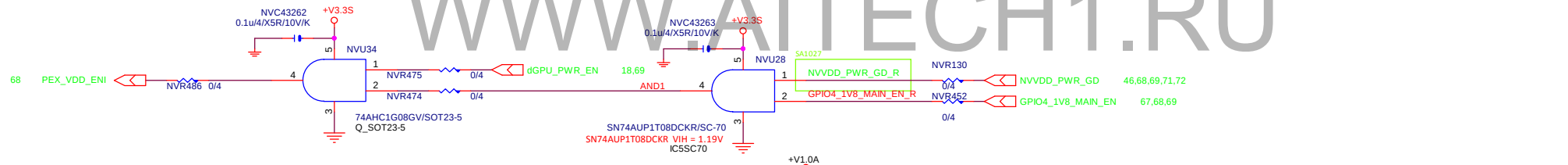
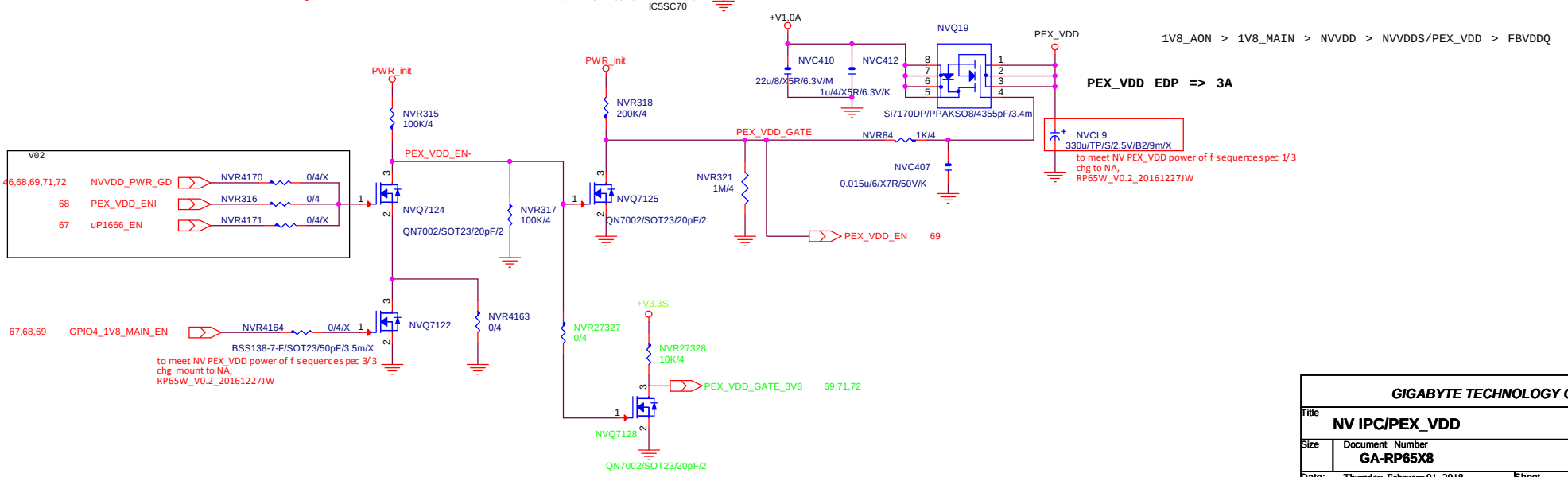


PEX_VDD

Power Monitor







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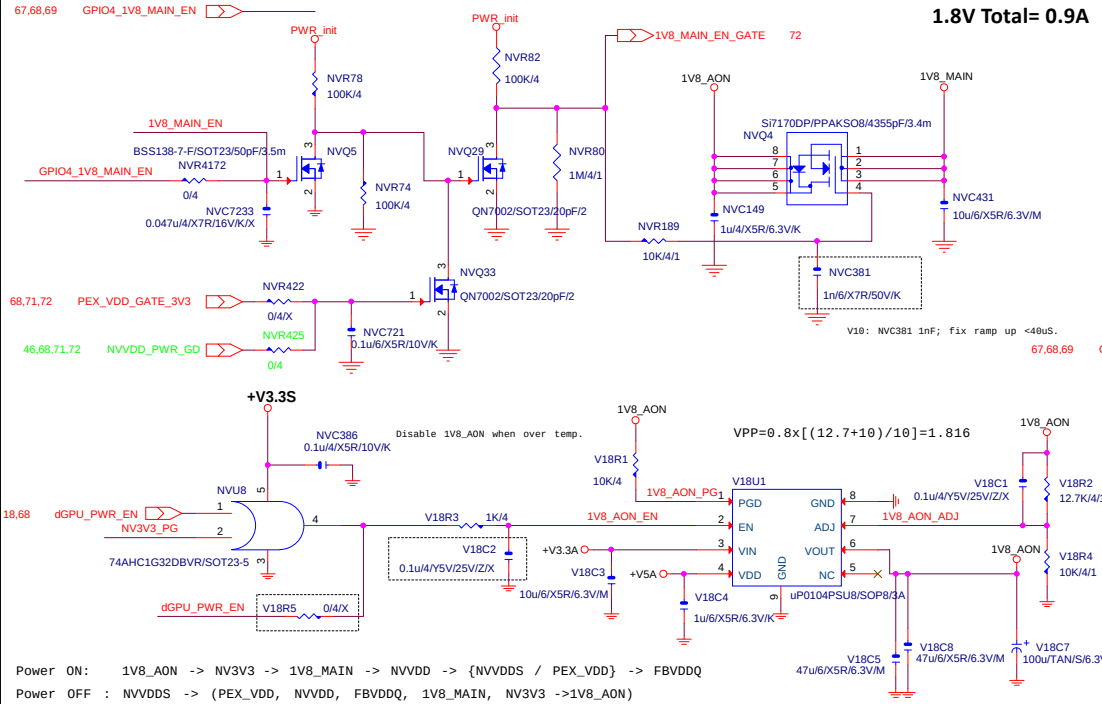
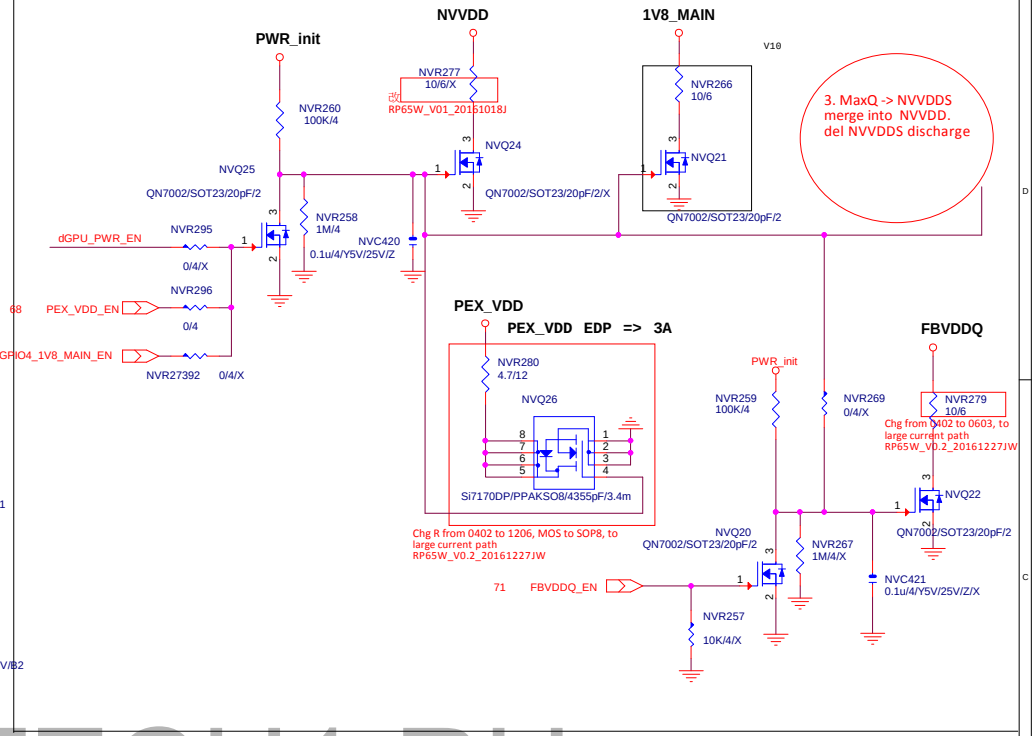
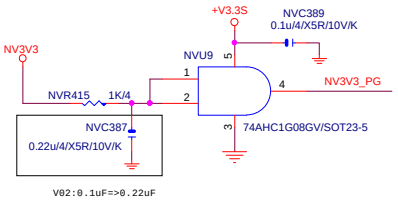
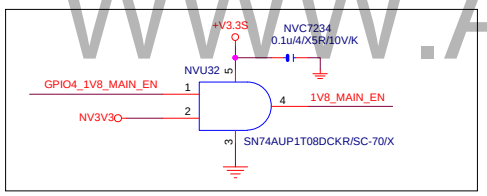








AE update new power sequence.
20161013

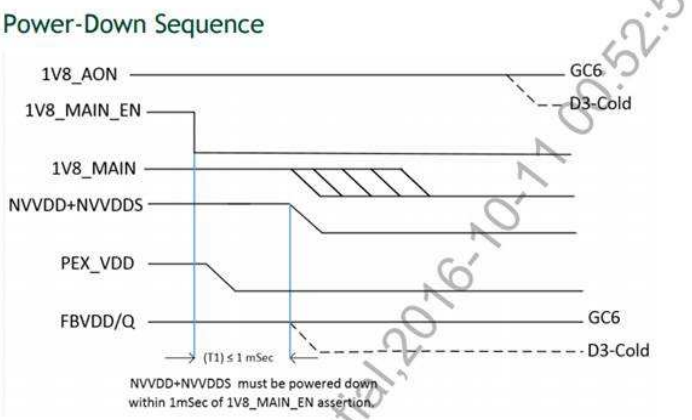
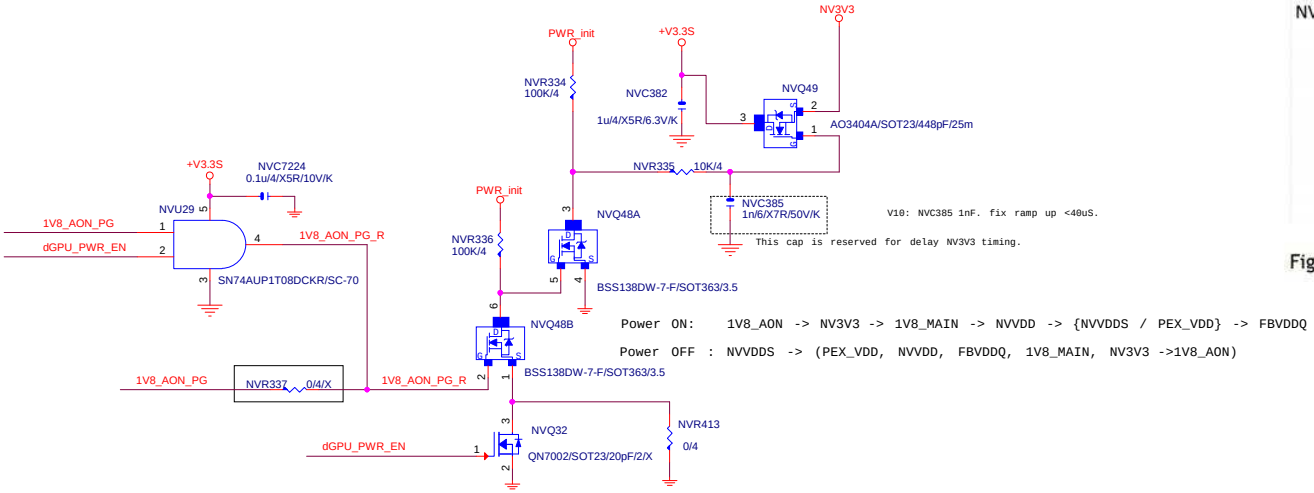


Figure 2. Example of Power-Down Sequencing Order



Power ON: 1V8_AON -> NV3V3 -> 1V8_MAIN -> NVVDD -> {NVVDDS / PEX_VDD} -> FBVDDQ
Power OFF : NVVDDS -> (PEX_VDD, NVVDD, FBVDDQ, 1V8_MAIN, NV3V3 ->1V8_AON)

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Title: NVVDDS			
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Power ON: 1V8_AON -> NV3V3 -> 1V8_MAIN -> NVVDD -> {NVVDDS / PEX_VDD} -> FBVDDQ

Power OFF : NVVDDS -> (PEX_VDD, NVVDD, FBVDDQ, 1V8_MAIN, NV3V3 ->1V8_AON)

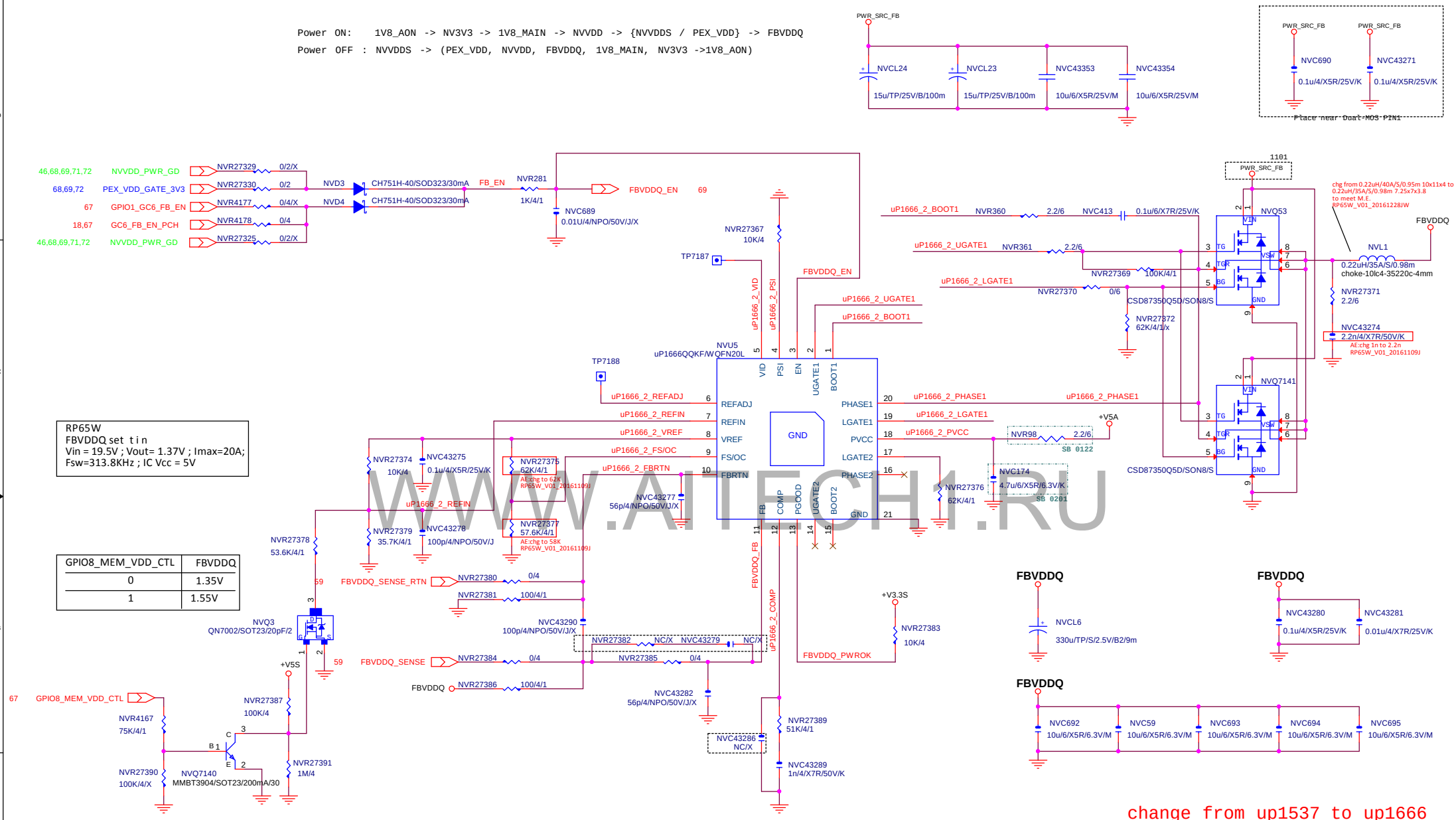

Table 11. Output EDP-Continuous

Product	TGP (W)	NVVDD NVVDDS - (A)	GPU FBIO (A)	FB TOTAL[5] (A)	1.0V Total[1] 1.0V[4] (A)	1.8V Total[2] 1.8V[4] (A)
N17E-G3 MAX-Q	80	76.4	17.1	32.8	0.8	1.6
N17E-G2 MAX-Q	80	79.1	14.6	25.0	0.8	1.6
N17E-G1 MAX-Q	60	62.8	12.6	19.8	0.8	1.6

Table 12. Output EDP-Peak

Product	TGP (W)	NVVDD NVVDDS - (A)	GPU FBIO (A)	FB TOTAL[5] (A)	1.0V Total[1] 1.0V[4] (A)
N17E-G3 MAX-Q	80	180	20.9	47.3	1.1
N17E-G2 MAX-Q	80	180	15.7	30.6	1.1
N17E-G1 MAX-Q	60	160	15.0	32.2	1.1

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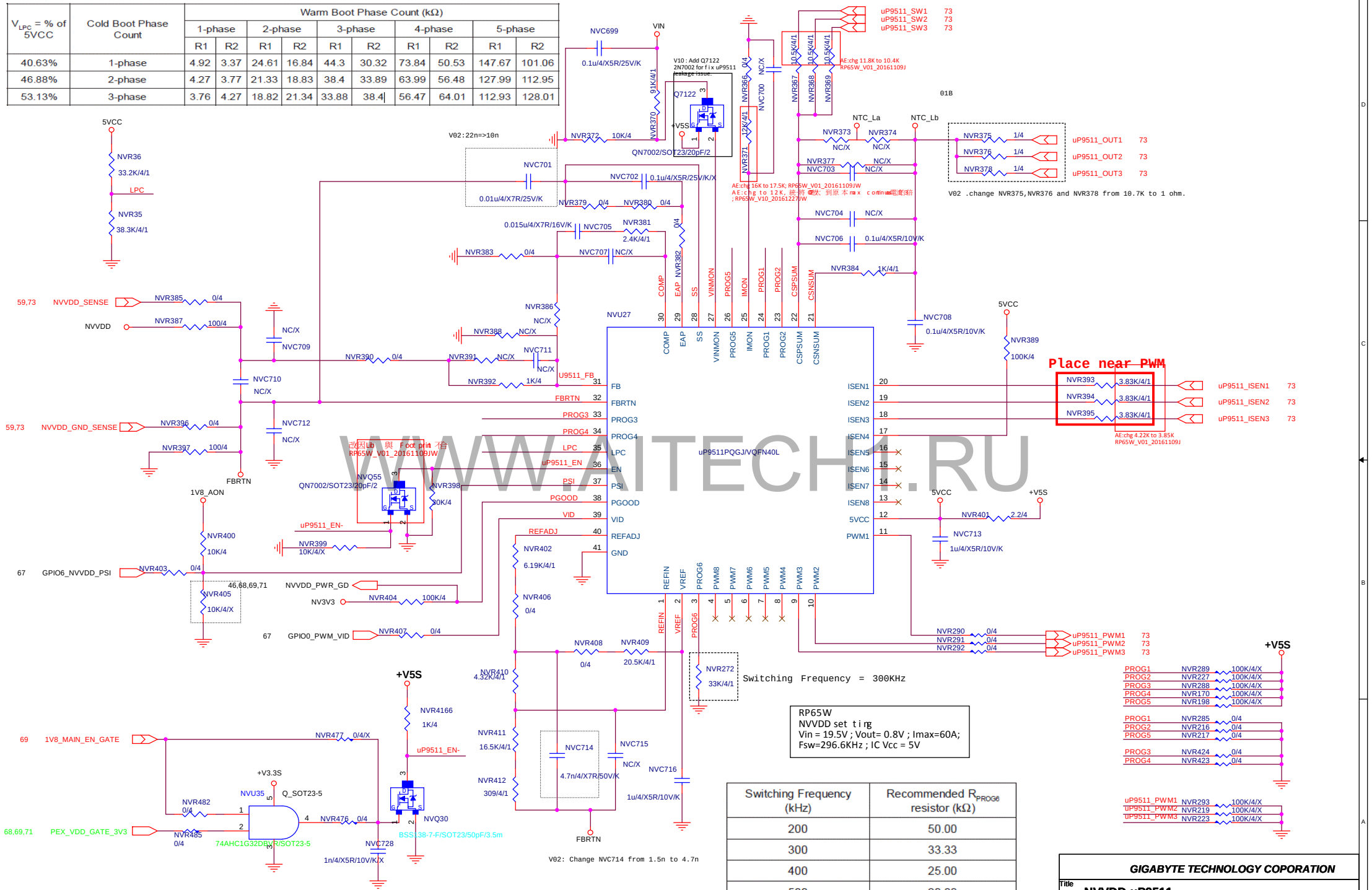
V_{LPC} = % of 5VCC	Cold Boot Phase Count	Warm Boot Phase Count (kΩ)									
		1-phase		2-phase		3-phase		4-phase		5-phase	
		R1	R2	R1	R2	R1	R2	R1	R2	R1	R2
40.63%	1-phase	4.92	3.37	24.61	16.84	44.3	30.32	73.84	50.53	147.67	101.06
46.88%	2-phase	4.27	3.77	21.33	18.83	38.4	33.89	63.99	56.48	127.99	112.95
53.13%	3-phase	3.76	4.27	18.82	21.34	33.88	38.4	56.47	64.01	112.93	128.01



RP65W
NVVDD set ting
Vin = 19.5V ; Vout= 0.8V ; Imax=60A;
Fsw=296.6KHz ; IC Vcc = 5V

Switching Frequency (kHz)	Recommended R_{PROG6} resistor (kΩ)
200	50.00
300	33.33
400	25.00
500	20.00
600	16.67

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Title: NVVDD-uP9511

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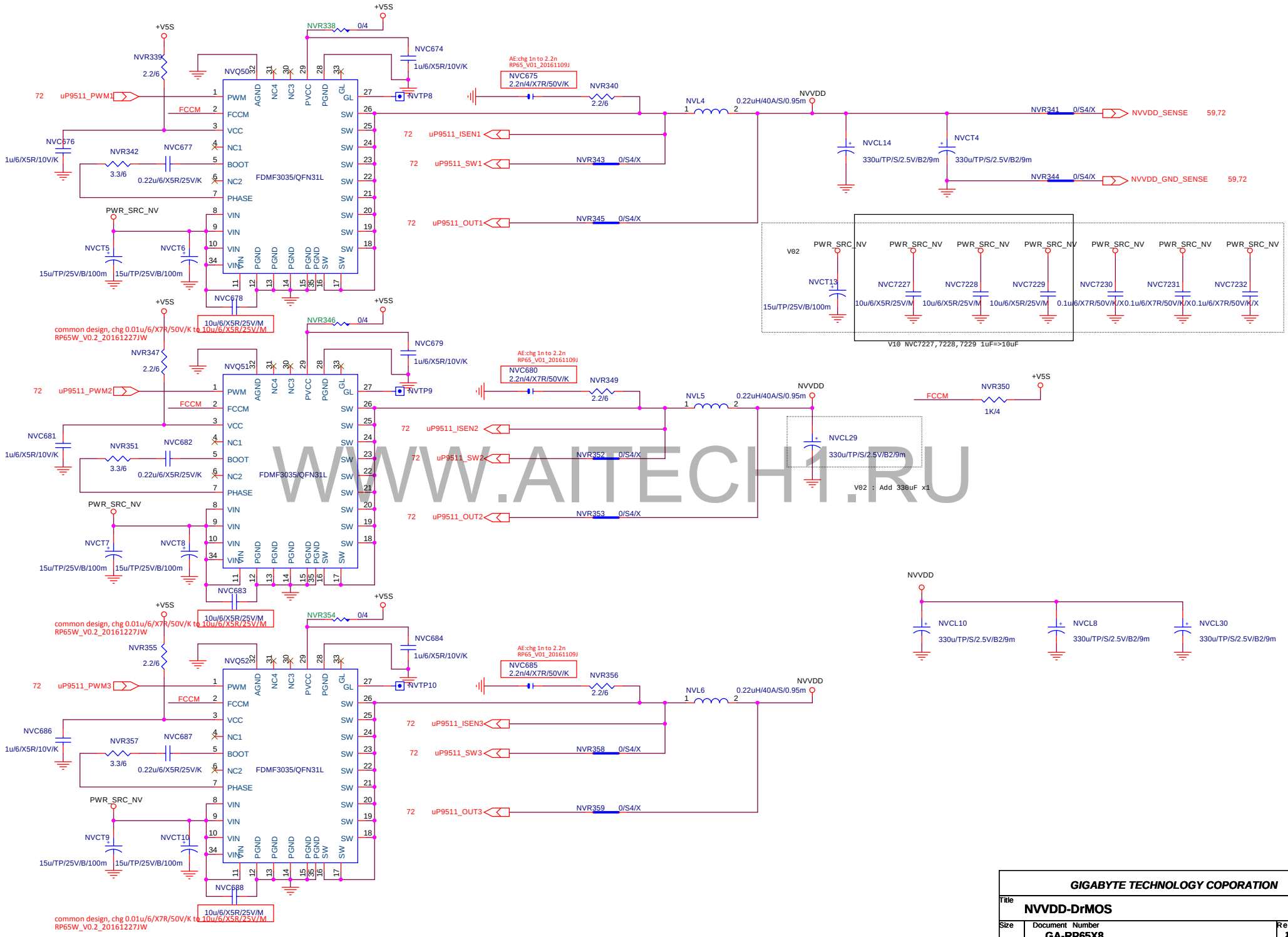

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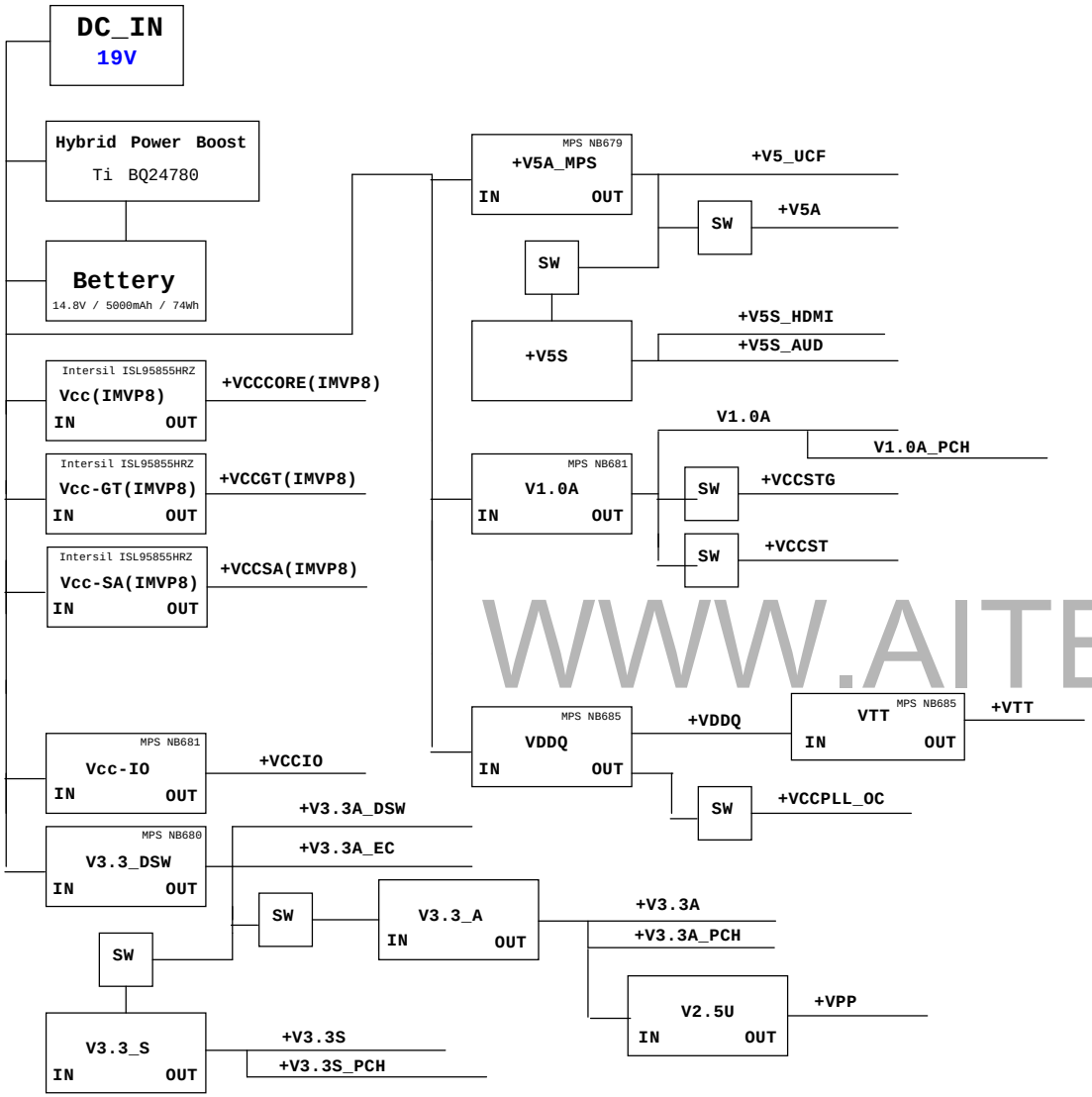
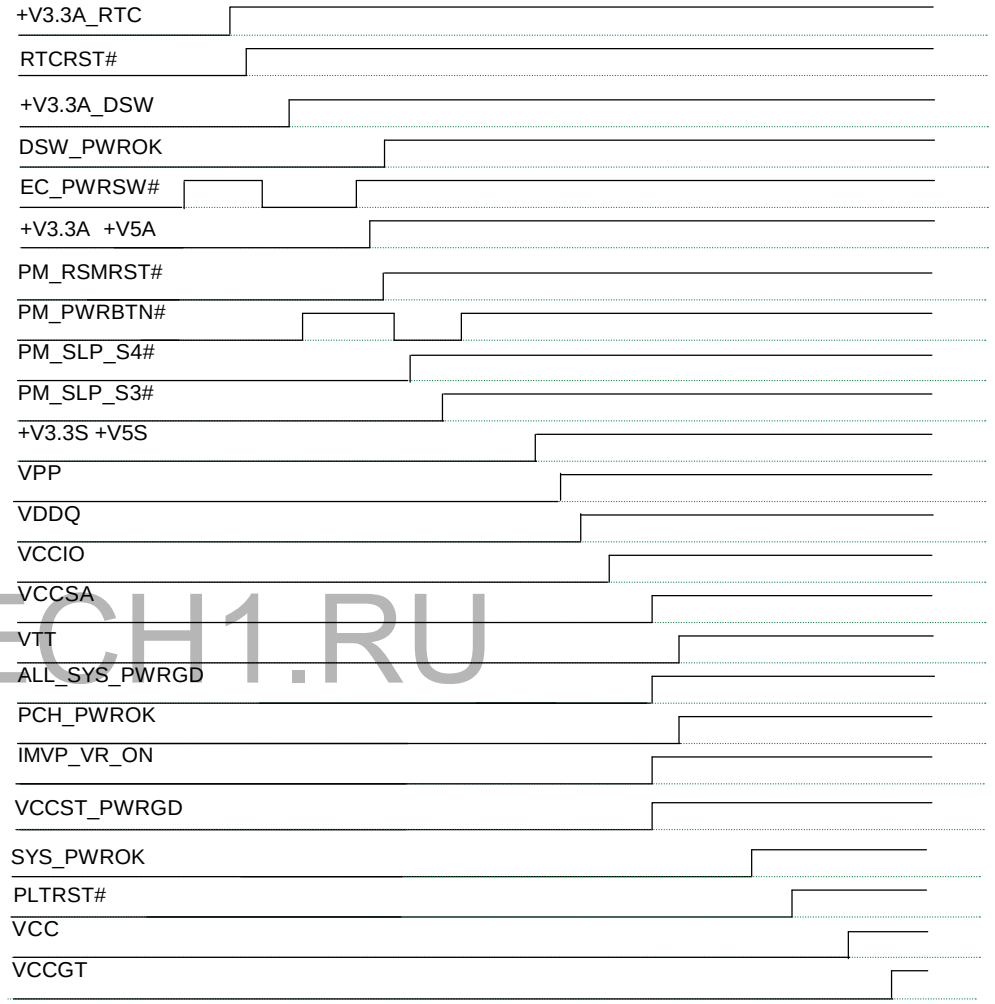
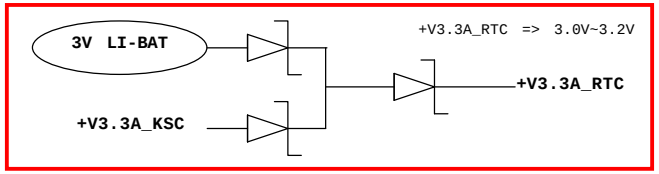


Powerup Sequence





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Title: Change_Note

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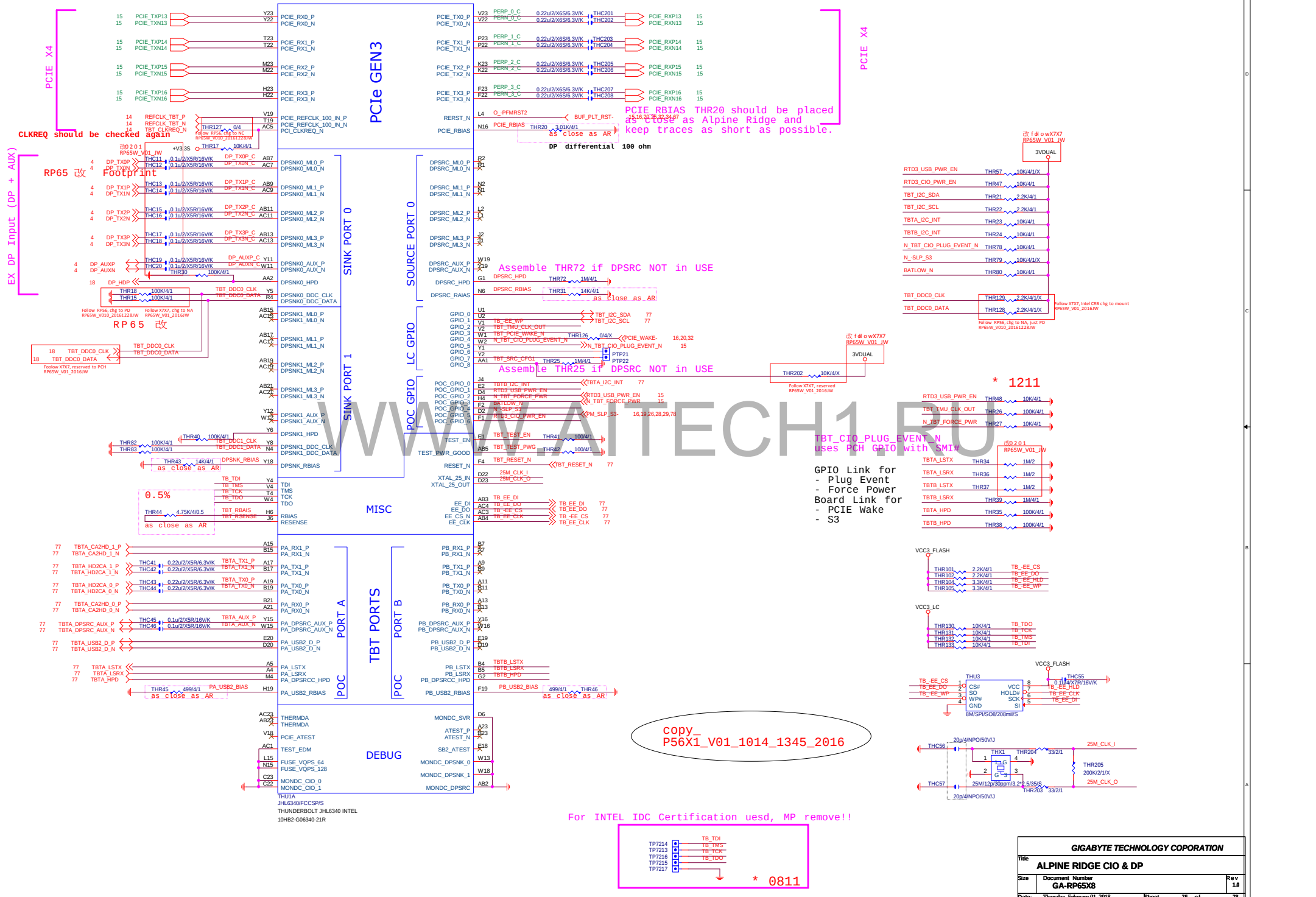
INTEL AR C version module (TBT + U31A) SCH 0.3 (2016/07/17) 4 Layers

Base on INTEL AR reference SCH 1.7 (2016/05/24)



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Title: ALPINE RIDGE CIO & DP			
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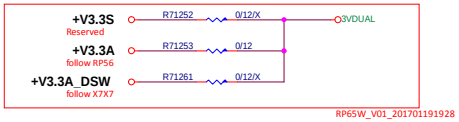
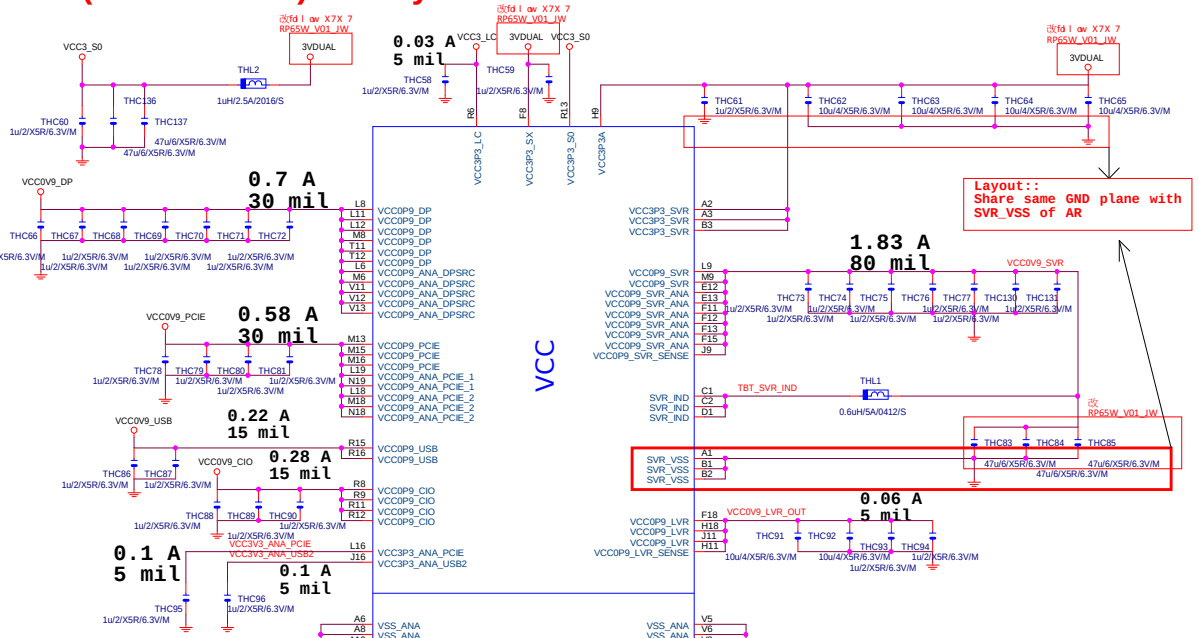
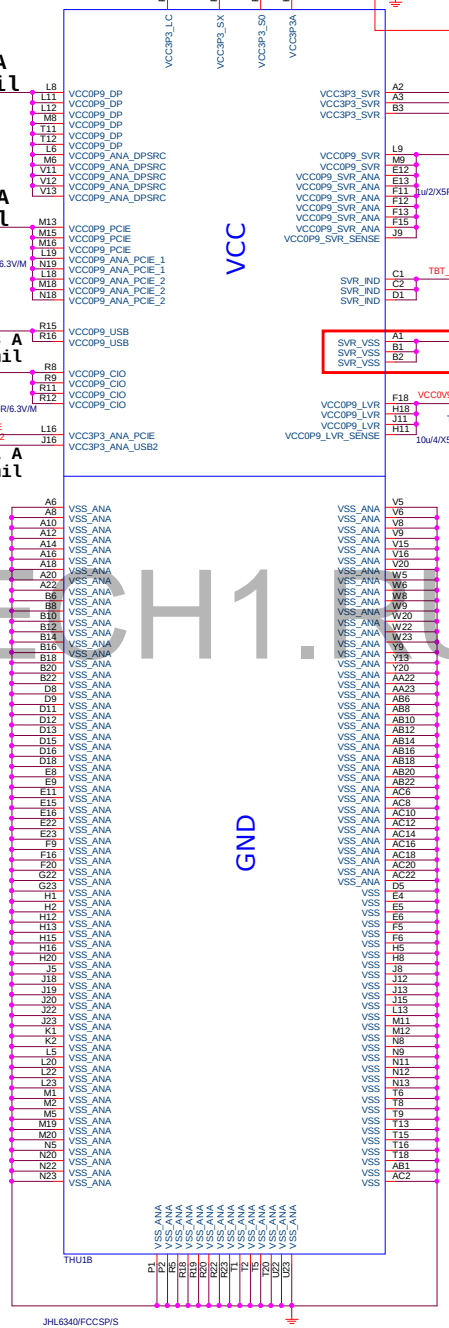
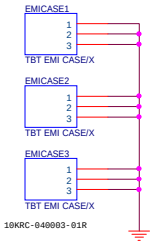
INTEL AR C version module (TBT + U31A) SCH 0.3 (2016/07/17) 4 Layers

Base on INTEL AR reference SCH 1.7 (2016/05/24)









VSS_ANA: VSS for Analog
VSS: VSS for Digital

Power Consumption Table					
	VCC3	3VDUAL	VCC3_LC	VCC3V3_ANA_PCIE VCC3V3_ANA_USB2	VCC0V9_LVR_OUT
Max Current(A)	1.05 A 40 mil	0.19 A 10 mil	0.03 A 5 mil	0.1 A 5 mil	0.06 A 5 mil
	VCC0V9_SVR	VCC0V9_DP	VCC0V9_PCIE	VCC0V9_USB	VCC0V9_CIO
Max Current(A)	1.83 A 80 mil	0.7 A 30 mil	0.58 A 30 mil	0.22 A 15 mil	0.28 A 15 mil

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JHL6340/FCCSP/S
THUNDERBOLT JHL6340 INTEL
10HB2-G06340-21R

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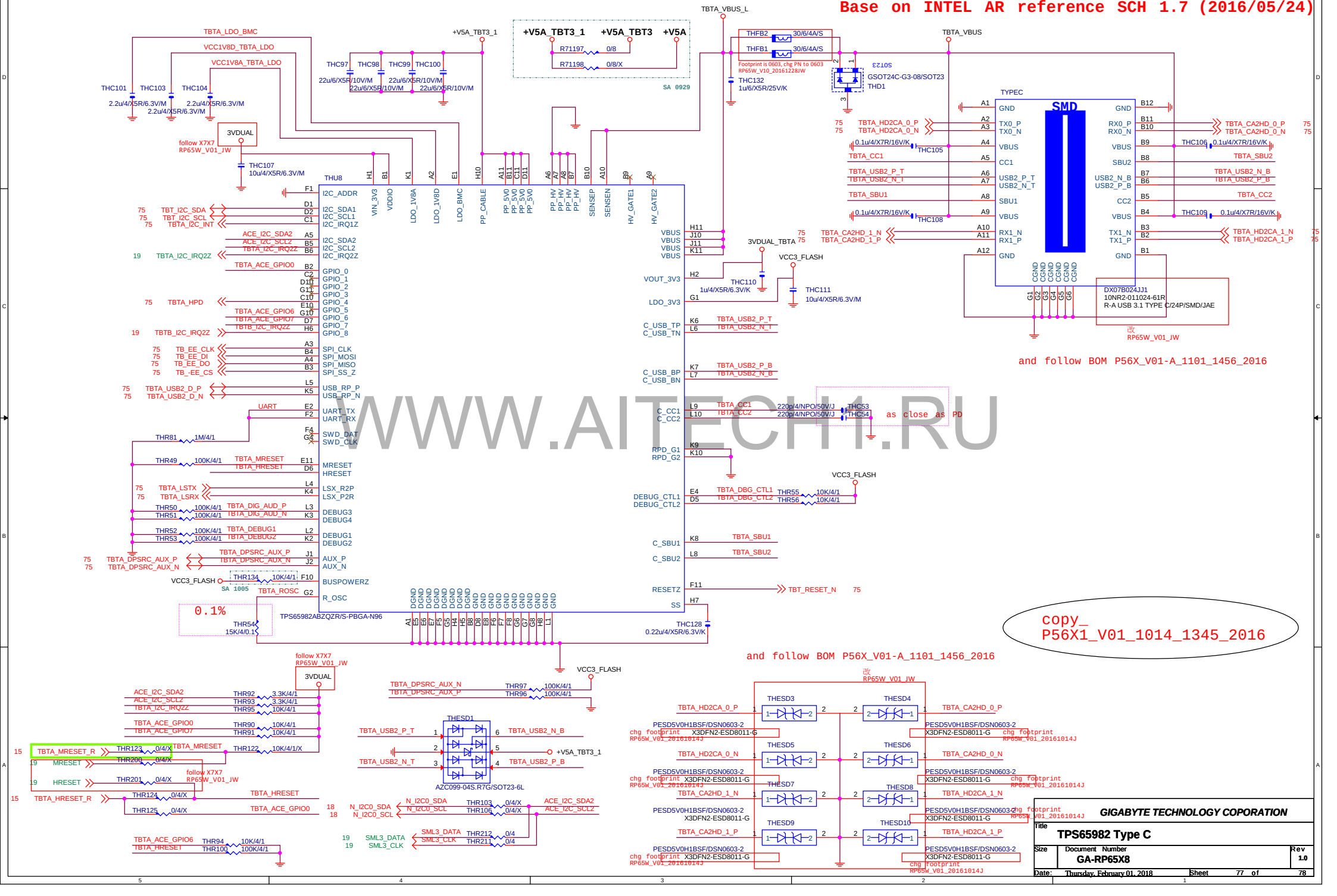
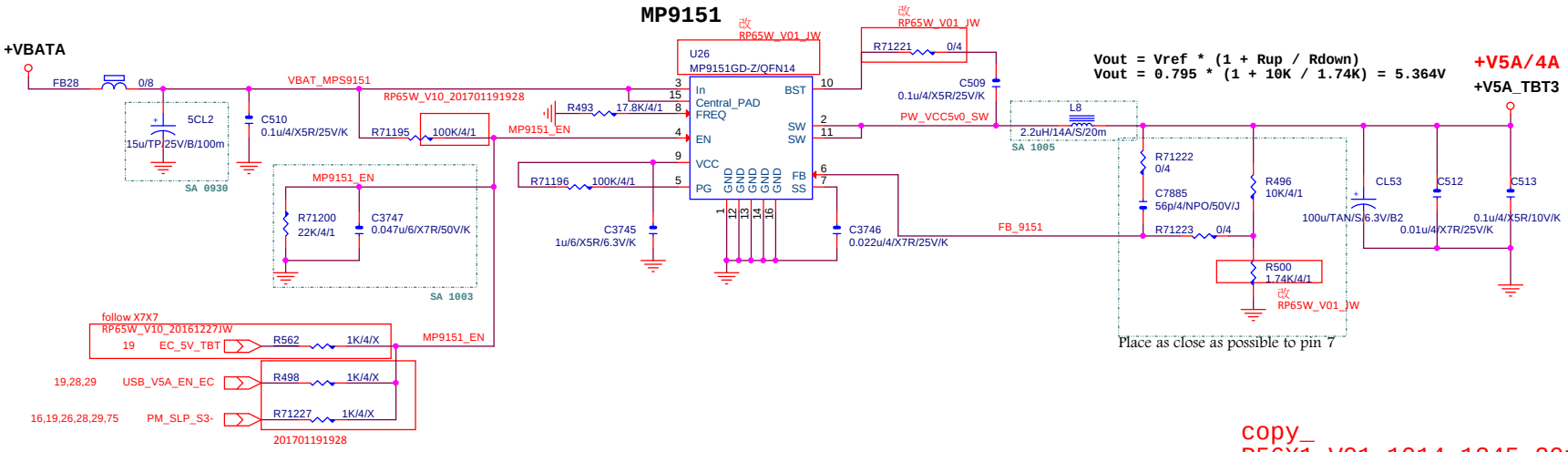
INTEL AR C version module (TBT + U31A) SCH 0.3 (2016/07/17) 4 Layers

Base on INTEL AR reference SCH 1.7 (2016/05/24)





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